Spin Dependent Transport in Semiconductor Nanostructures

Yilmaz Gul

Department of Electrical & Electronic Engineering

University College London

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I would like to dedicate this thesis to my loving parents

Declaration

This dissertation is the result of my own work carried out between October 2013 and September 2017 in the London Centre for Nanotechnology at UCL, Semiconductor Physics Group at the Cavendish Laboratory and the Cambridge Research Laboratory of Toshiba Research Europe Limited, and includes nothing which is the outcome of work done in collaboration, except where otherwise acknowledged. It has not been submitted in whole or part for a degree at this or any other University. It is less than hundred thousand words in length.

Yilmaz Gul, September 2017

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Abstract

This project investigates transport properties of electrons and holes confined into one-dimensional regions using lithographically patterned surface gates in $In_{0.75}Ga_{0.25}As$ and p-type Ge quantum wells respectively. A series of transport experiments was conducted to investigate many body effects in electrons and holes in one dimension. The experimental results provided here show important advances in both $In_{0.75}Ga_{0.25}As$ and p-type Ge quantum wires and lays the ground work for future experiments for spintronics research using these materials.

The first experiments reported here (chapter 4) describes the experiments carried out to optimise fabrication methods and determine the ideal length scales of split gates to observe clear ballistic transport features in high mobility $In_{0.75}Ga_{0.25}As$ wafers.

The following chapter (chapter 5) summarises the one dimensional transport measurements carried out on narrow split gates fabricated on the high mobility $In_{0.75}Ga_{0.25}As$ quantum wells. It explores how Rashba spin orbit coupling effects the transport properties. In $In_{0.75}Ga_{0.25}As$ a weaker backscattering due to the time-reversal asymmetry in the one-dimensional channel results in enhanced ballistic transport characteristics with clear quantised conductance plateaus up to $6(2e^2/h)$. We investigate the conductance data when a d.c. voltage is applied to the source and the drain contacts and a method for obtaining the effective g factor is described.

Chapter 6 introduces p-type Ge, and summarises one dimensional transport properties of these devices. We demonstrate quantised conductance up to 10 $(2e^2/h)$. Applied source-drain voltages and symmetric gating of the channel has uncovered plateau at half integer values as well as ballistic structure down to $0.25(2e^2/h)$. These systems also show a ballistic plateau at 0.25 $(2e^2/h)$, when the carrier density is reduced using a top gate electrode.

The last experimental chapter (chapter 7) analyses the many-body effects observed in one-dimensional transport measurements in p-Ge and analysis

of anomalous 0.25 ($2e^2/h$) plateau is provided with possible explanations for it. We have also shown that we can alter the confining potential using lateral gate voltages to create a row formation as the ground state effectively creates a Wigner lattice.

Impact Statement

This thesis provides advances in transport properties of electrons in InGasAs and show very clean conductance plateaus for the first time for this material. The spin-orbit coupling interestingly seems to enhance the ballistic nature by plateaus up to much higher values of conductance than reported before. This will be a boost to the field of transport through InGaAs which is important because of the anticipated applications of spin-orbit interactions in spintronics.

The work presented in this thesis also shows the existence of fractional quantisation and possible fractional charge. Chapter 7 presents potentially ground-breaking results: fractional charges in transport. These have been obtained by tuning the effect of the interactions strong in the hole gas by depletion and weakening the confinement. The work presented in this thesis will stimulate a wide range of disciplines in addition to condensed matter physics, for example semiconductor growth and use of Ge in new solid state devices.

Germanium is fully compatible with silicon, and the two elements can be integrated using modern semiconductor technologies. The fact that this phenomenon occurs in the absence of a magnetic field enables control circuitry to be installed on a silicon chip so allowing the development of an integrated quantum computer on a single silicon chip. In addition, the fact that the effect occurs spontaneously opens the door to tailoring the confinement of both electrons and holes in a controlled manner to attempt to control the value of the effective charge of the current carrying species. This has important implications for a wide range of developments in information technology.

This project has laid the ground work needed for fabricating more complex

devices on both $In_{0.75}Ga_{0.25}As$ and p-Ge. We have optimised the fabrication methods that are suitable for fabricating more complex devices.

Publications

The work described in this thesis has resulted in the following publications:

Y. Gul, G. L. Creeth, D. English, S. N. Holmes, K. J. Thomas, I. Farrer, D. J. Ellis, D. A. Ritchie, and M. Pepper *Conductance quantisation with Rashba spin-orbit coupling in* $In_{0.75}Ga_{0.25}As$ *quantum wires* - To be published.

Y. Gul, S. N. Holmes, P. J. Newton, D. J. P. Ellis, C. Morrison, M. Pepper, C. H. W. Barnes and M. Myronov *Quantum ballistic transport in epitaxial, strained Germanium* Appl. Phys. Lett. 111 233512, 2017

Y. Gul, S. N. Holmes, S. Kumar , M. Pepper, and M. Myronov *Self-organised fractional quantisation in a hole quantum wire* J. Phys.: Condens. Matter 30 09LT01, 2018

Kaveh Delfanazari, Rueben K Puddy, Pengcheng Ma, Teng Yi, Mode Can, Yilmaz Gul, Ian Farrer, David A Ritchie, Hannah J Joyce, Michael J Kelly. *On-Chip Andreev Devices: Hard Superconducting Gap and Quantum Transport in Ballistic Nb-*$In_{0.75}Ga_{0.25}As$ *Quantum Well-Nb Josephson Junctions* - Advanced Materials, 2017

Work presented at conferences

UK Semiconductors - Sheffield - July 2016 -Poster - Y. Gul, S. N. Holmes, P. J. Newton, D. J. P. Ellis, C. Morrison, M. Pepper, C. H. W. Barnes and M. Myronov *Quantised Conductance in p-type Ge.*

International Conference on Physics of Semiconductors (ICPS)- Beijing/China August 2016 - Oral Presentation- Y. Gul, S. N. Holmes, P. J. Newton, D. J. P. Ellis, C. Morrison, M. Pepper, C. H. W. Barnes and M. Myronov. *Quantised conductance in p-type Ge.*

Physics and Applications of Spin-Related Phenomena in Solids (PASPS) - Kobe/Japan August 2016 - Poster- Y. Gul, G. L. Creeth, D. English, S. N. Holmes, K. J. Thomas, I. Farrer, D. J. Ellis, D. A. Ritchie, and M. Pepper *Conductance quantisation in* $In_{0.75}Ga_{0.25}As$ *at 50 nm Length Scales.*

International Conference on Silicon Epitaxy and heterostructures (ICSI) - Warwick/UK May 2017 - Oral Presentation: Y. Gul, S. N. Holmes, P. J. Newton, D. J. P. Ellis, C. Morrison, M. Pepper, C. H. W. Barnes and M. Myronov. *Quantum ballistic transport in strained epitaxial p-type Ge.*

Advances in Quantum Transport in Low Dimensional Systems - London September 2017 - Poster- Y. Gul, G. L. Creeth, D. English, S. N. Holmes, K. J. Thomas, I. Farrer, D. J. Ellis, D. A. Ritchie, and M. Pepper *Conductance quantisation with Rashba spin-orbit coupling in* $In_{0.75}Ga_{0.25}As$ *quantum wires.*

Contents

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List of Abbreviations and variables

0D	Zero-Dimensional
1D	One-dimensional
2D	Two-dimensional
2DEG	Two-Dimensional Electron Gas
2DHG	Two-Dimensional Hole Gas
d.c	Direct Current
a.c	Alternating Current
InGaAs	Indium Gallium Arsenide
InAlAs	Indium Aluminium Arsenide
Ge	Germanium
GaAs	Gallium Arsenide
SiGe	Silicon Germanium
AuGeNi	Gold Germanium Nickel
Al	Aliminum
DOS	Density of States
QW	Quantum Well
HH	Heavy Holes
LH	Light Holes
HEMT	High Electron Mobility Transistor
g	Electron g-factor
^{4}**He**	^{4}Helium isotope
^{3}**He**	^{3}Helium isotope
J, $\mathbf{J}_z$	Total angular momentum operator
$m*$	effective mass
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
$\mathbf{N}_2$	Nitrogen

QPC	Quantum Point Contact
QW	Quantum Well
UV	Ultra Violet
UHV	Ultra High Vacuum
RTP	Rapid Thermal Annealer
VTI	Variable Temperature Insert
PECVD	Plasma Enhanced Chemical Vapour Deposition
RHEED	Reflection High Energy Electron Diffraction
UCF	Universal Conductance Fluctuations
DI	De-Ionised
MIBK	Methyl Isobutyl Ketone
MEK	Methyl Ethyl Ketone
SdH	Shubnikov-De Hass
FFT	Fast Fourier Transform
SOI	Spin Orbit Interaction
BIA	Bulk Inversion Asymmetry
SIA	Structural Inversion Asymmetry
PMMA	polymethylmethacrylate
SEM	Scanning Electron Microscope
CRL	Cambridge Research Laboratory (Toshiba)
HCL	Hydrochloric Acid
RF	Radio Frequency
IPA	Isopropanol
LED	Light Emitting Diode
LOR	Lift Off Resist
MBE	Molecular Beam Epitaxy
RP-CVD	Reduced Pressure - Chemical Vapour Deposition

Chapter 1

Introduction

The introduction of the integrated circuit in the late 1950's, after the first transistor was made by Bardeen and Brattain in 1947, has caused a revolution in the development of modern computers. Integrated circuits (IC) contains a large number of transistors, since their introduction, the number of individual transistors in a single IC have roughly doubled each year. This was observed by the co-founder of Intel in 1965, and has been roughly true since (Moore's Law). Moore's Law was an economical observation, as the unit costs went down the number of transistors in IC was expected to double every year. In 1980 Hewlett-Packard produced a single-chip microprocessor containing approximately 0.5 M transistors in 1 cm^2 area [1], with transistors having a nominal 1.25 μm gate length, this was considered an incredible step forward. In 2016 mass production of 10 nm devices have started and first shipments is expected to be made in the first quarter of 2017. However the 7 nm scale as defined by International Technology Road Map of Semiconductors ITRS [2] is seen as the end of Moore's law. The current transistors has nearly reached its fundamental constraints, this is due to quantum mechanical effects associated with electrons in confined systems. As a consequence there is a vast research going on for exploiting the tremendous power of the possibilities of quantum computing [3].

There has been ongoing research on Group III - Group V (III-V) semiconductors especially on Gallium Arsenide (GaAs) and Aluminium Arsenide (AlAs) for over thirty years. The research have been centred on high quality materials, fabricating similar size structures but designed and investigated under conditions that allow for quantum effects to dominate its properties, usually requiring cryogenic temperatures. Many fundamental properties have been observed such as the quantisation of conductance [4], the quantum Hall Effect [5], the Aharonov-Bohm effect [6] and the Coulomb-Blockade

effect [7].

The main focus of this project is to make use of these quantum features to use as a platform to explore potential new physics, as well as making use of the strength of spin-orbit interaction in the case of $In_xGa_{1-x}As$ wafers and the effect of hole-hole interactions in the case of recently grown epitaxial Ge quantum wells.

Using electron spin to store logical information also paves the way for quantum computing [8]. Exploitation of quantum phenomena to store and perform computational operations on data was first suggested by Richard Feynman [9]. Classical computational operations are performed by using series of binary bits in one of two distinct states: 0 and 1. However quantum mechanics allow, quantum bits (qubits) to exist in states 0 or 1, and also in a superposition of two states. The system may exist in all theoretically possible states simultaneously according to a linear combination of basis states ($|0\rangle$ and $|1\rangle$). The basis states is associated with a probability amplitude of α and β. Hence a qubit may exist in the superposition $\psi = \alpha|0\rangle + \beta|1\rangle$. However superposition is not an observable quantity, and will collapse to $|0\rangle$ or $|1\rangle$ upon measurements depending on the probability amplitudes α and β. The superposition makes a quantum computer capable of performing any computation by probabilistically sampling all linear combinations of states at once [3], which a classical computer lacks. Algorithms have been proposed to be used in quantum computation to exponentially speed up factorisation [10], and to solve problems that cannot otherwise be tackled efficiently using a classical computer. Quantum computers must fill several criteria detailed by Loss and DiVencenzo [11, 12]. There are as follows:

- Scalable physically to increase the number of qubits.
- Qubits that can be initialised to arbitrary values.
- Quantum gates that are faster than decoherence time (around tens of femtoseconds [13]).
- Universal gate set, such as the application of a controlled NOT (CNOT) logic gate for an electron spin flip [14].
- Qubits that can be read easily.

Only one of these criteria actually rely on quantum effects, the ability for arbitrary unitary transformation, which requires the ability of mixing of the two possible states within a qubit as an arbitrary superposition, and also entanglement between qubits.

Among many implementations suggested for quantum computing, the most important attempt is through semiconductor nanostructures. Semiconductors are attractive due to their robustness and their apparent scalability, but most importantly the ability to incorporate manufacture of such devices into existing industrial infrastructures. Electron spin is being considered to be used as a qubit. However many challenges must be overcome, such as injection, manipulation and detection of spin-polarised current purely electronically. For this to be achieved materials with high spin-orbit coupling are being investigated, as spin-orbit coupling is a possible tool for electrical spin injection and control without ferromagnetic contacts or applied magnetic fields. Rashba spin-orbit coupling [15, 16] could achieve electrical spin control and generation of spin polarised current without the use of ferromagnetic contacts [17]. The Rashba spin-orbit coupling effect arises when electrons move in an asymmetric potential generated at the interface of a heterojunction or in a quantum well, an effective magnetic field in the rest frame of the moving electron arises as a result of the net electric field that exists perpendicular to the interface. The effective Rashba magnetic field, which lies in the plane of the 2DEG, lifts the spin degeneracy of the carriers. This in turn results in the precession of the spin vector, the frequency of which precession could be modulated by adjusting the gate voltage to tune the confinement potential at the heterointerface [15]. $In_xGa_{1-x}As$ systems exhibit strong Rashba spin-orbit coupling, resulting in a finite spin-splitting energy (ΔE_S) at low magnetic fields and a band structure dominated by Bychkov-Rashba spin-orbit coupling induced by structural inversion asymmetry (SIA) [18] at zero magnetic field [19]. $In_{0.75}Ga_{0.25}As$ and $In_{0.75}Al_{0.25}As$ are interesting compounds due to the lower effective mass of electrons ($m^* = 0.040m_e$ versus $m^* = 0.067m_e$ in GaAs) [20], which results in high peak electron velocities for a given field electron density, high low-field electron mobilities and increased electron subband energy spacing [21].

In this project we have worked with two distinct material systems, $In_{0.75}Ga_{0.25}As$ with strong Rashba spin orbit coupling and high mobility p-Ge with no Rashba field in 1D and negligible spin orbit coupling.

The ITRS has identified p-Ge as a candidate for channel replacement material in p-MOS and the ballistic transports measurements presented in this project not only strengthens the case for Ge inclusion in the ITRS but also demonstrates that p-Ge has device potential for nanoelectronics and quantum computing applications.

Chapter 2

Transport in Nanostructures

2.1 Semiconductor crystals

Semiconductors have periodic crystal lattices. III-V semiconductors such as GaAs, InAs, AlAs, GaSb etc. have a zincblende structure while silicon and germanium crystallise in the diamond lattice, which is a repeating pattern of 8 atoms, this structure makes them much more stronger than zincblende structures.

The zincblende lattice is a diamond lattice, an fcc lattice with a basis consisting of two atoms of the same kind (Fig 2.1), but for the zincblende lattice two atoms forming the basis of the fcc lattice are different. The room temperature lattice constants a for GaAs, AlAs and InAs are, 5.6533 Å, 5.6605 Å, and 6.0583 Årespectively [22]. The lattice match between GaAs and AlAs paves the way for growing thick layers of $Al_xGa_{x-1}As$ with very little strain. As a result of this complex heterostructures can be grown for bandgap engineering. The transition from direct to indirect bandgap is close to x= 0.45 in $Al_xGa_{x-1}As$.

Similarly the band gap energy (E_g) of $In_xGa_{x-1}As$ can be tuned with In mole fraction by [23],

$$E_g = 1.42 - 1.615x + 0.555x^2 \tag{2.1}$$

The lattice constants a of $In_xGa_{1-x}As$ and $In_yAl_{1-y}As$ vary with In mole fraction by:

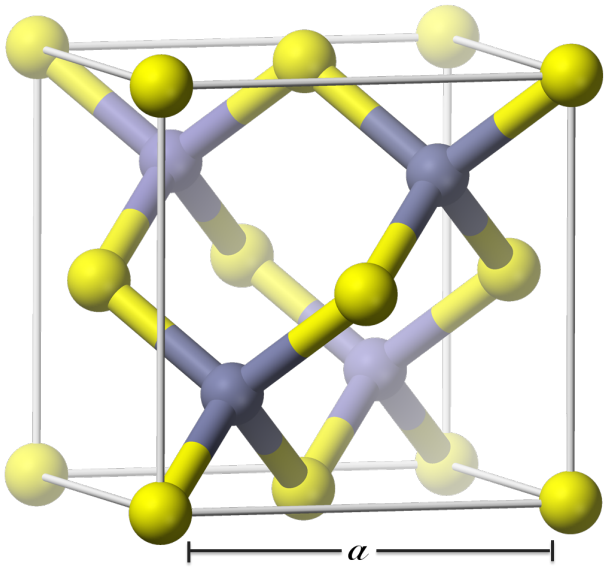

Figure 2.1: Shows the zinc-blende crystal structure, a is the lattice constant given by the size of the cubic unit cell.

$$a = 0.405x + 5.6533 \tag{2.2}$$

$$a = 0.3978y + 5.6605 \tag{2.3}$$

Which can be used to give experimental approximations for the variation of the lattice constant a [22].

2.2 Bandgap Engineering

A bandgap is the range in a solid where no electron states can exist, this is very large in insulators and very small or nonexistent in conductors, as the valence and conduction band overlaps. In semiconductors the band gap can be engineered using a variety of techniques to create desirable electrical properties. One way to do this is using molecular beam epitaxy (MBE) to grow layers of different semiconductors with high precision, mono-layer degree of control in growing such structures. By increasing the

number of available charge carriers by doping, it is possible to modify the characteristics of the structures. This can be carried out by either incorporating donor impurities which leads to extra conduction electrons or acceptor impurities to have additional holes. Varying the composition of the material alters the band gap due to bonding of different atoms with different energy level gaps. Lattice mismatch is another way to alter the band-gap by introducing strain [24]. In this project heterostructures of InGaAs grown by MBE and low defect Ge system with SiGe barriers grown by reduced pressure chemical vapour deposition (RP-CVD) have been used.

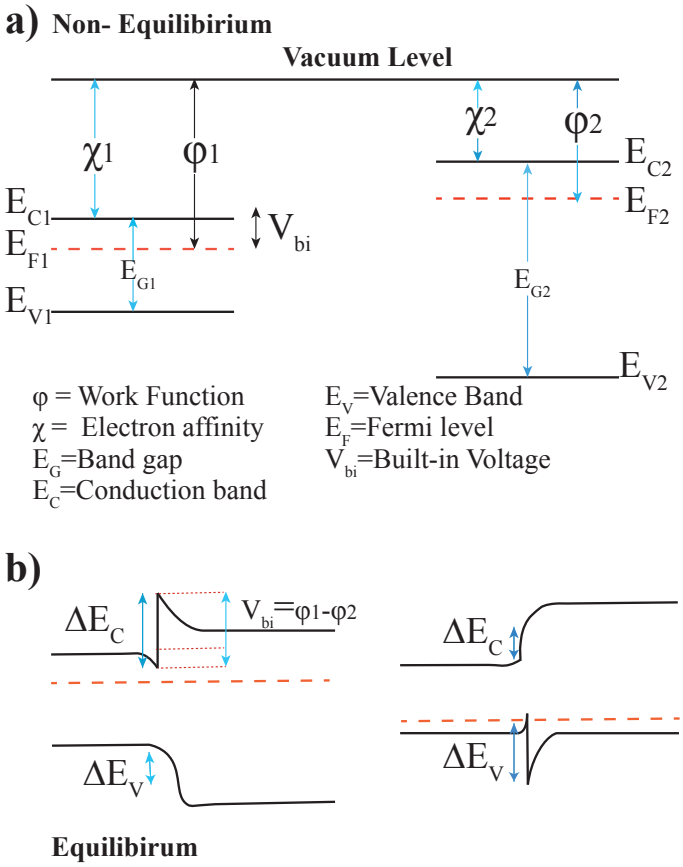

Figure 2.2: **a)** Band structure of two semiconductors at a heterojunction interface before equilibrium. **b)** *Left:* After equilibrium for electrons *Right:* After equilibrium for holes.

Figure 2.2a shows a typical band structure of two dissimilar semiconductors at a

heterojunction interface, where the band structure of each layer is dependent on the relative bandgaps E_G, as well as electron work functions of each material. In equilibrium charge flows from one material to the other, thus areas vacated become positively charged and where charge accumulates becomes negatively charged for electrons and vice versa for holes. It is this imbalance of charge that results in band bending (figure 2.2b).

2.3 Density of States

The characteristics of semiconductors are primarily determined by their band-structure and their density of states. The density of states (DOS), describes the number of states N per interval of energy (E) at each energy level that are available to be occupied, per unit volume. The density of conduction states, ρ(E), is given by

$$\rho(E) = \frac{dN(E)}{dE} \tag{2.4}$$

The density of states in zero magnetic field for electrons in 3D, 2D, 1D and 0D are as follows

$$\rho_{3D}(E) = \frac{m*}{\pi h^2}\frac{\sqrt{2m*E}}{\pi\hbar} \tag{2.5}$$

$$\rho_{2D}(E) = \frac{m*}{\pi h^2} \tag{2.6}$$

The density of states for a spin-degenerate, two-dimensional electron gas is given by

$$\rho_{2D}(E) = \frac{n(E)m*}{\pi h^2} \tag{2.7}$$

where $n(E)$ is the integer number of accessible quantised energy levels (subbands).

$$\rho_{1D}(E) = \frac{m*}{\pi h^2}\frac{2\hbar}{\sqrt{2m*E}} \tag{2.8}$$

$$\rho_{0D}(E) = 2\delta(E) \tag{2.9}$$

where m* is the effective mass of electron. In the above equations only the density of states in 2D is independent of energy.

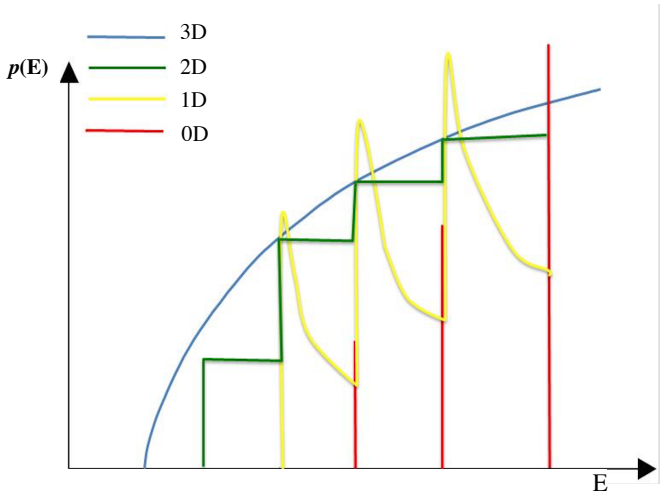

Figure 2.3: Density of electronic state functions for different confinements.

The density of states for holes in the valence band is given by:

$$\rho_V(E) = \frac{8\pi\sqrt{2}}{h^3} m_h^{*3/2} \sqrt{E_V = E}, \text{for } E \leq E_V, \tag{2.10}$$

where m_h^* is the effective hole mass.

Figure 2.3 shows the shape of the density of states for the four confinement situations.

2.4 Electron Transport in Two-Dimensions

Most low-dimensional nanostructures use a two-dimensional electron gas (2DEG) or for p type semiconductors two-dimensional hole gas (2DHG) as a starting point. To obtain a 2DEG/2DHG, semiconductor heterostructures are used; these are composed of layers of different types of semiconductors. In this project a heterostructure based around $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ was used to create a high-electron-mobility transistor (HEMT) based on a 30 nm of quantum well (QW). In the later part of the project we have used Ge quantum well sandwiched between $Si_{0.3}Ge_{0.7}$ with a Ge Cap layer. Both systems required electrically insulating layer at the interface between the semiconductor and the metal gates, which increases the Schottky barrier height, to stop leakage currents.

2.4.1 Two-dimensional Electron Gas

In order to achieve a 2DEG, free electrons are confined into a two-dimensional sheet. A common heterostructure is GaAs/AlGaAs HEMT, the first observation of 2DEG in GaAs/AlGaAs heterostructure was reported by Störmer *et al.* [25] in 1979, using this structure electron mobilities above 30 million $cm^2V^{-1}s^{-1}$ have been demonstrated [26]. An example of a band structure of GaAs/AlGaAs heterostructure is shown in figure 2.4.

At temperatures above $\sim$ 100K, the electrons from the Si-doped AlGaAs layer are free to move around various layers but still close to their ionised donors due to Coulomb interactions. The electrons can be thermally activated over the small barrier in the conduction band edge into the GaAs conduction band. At temperatures below $\sim$ 100K the electrons are lower in energy and are trapped in a triangular quantum well. This is induced by the conduction band discontinuity and the Coulomb interactions between the ionised donors and electrons. As a result the motion of electrons in the z-direction is therefore restricted, while the electrons can still move freely on the $x-y$ plane of the interface, therefore they are confined in a two-dimensional system.

2.4.2 Two-dimensional Hole Gas

Similar to electrons, an effective confinement of holes in the valence band of a quantum well is also possible, and in this project we have worked with Ge quantum wells in SiGe heterostructures, in which the Ge quantum well is strained due to lattice mismatch. However the description of two-dimensional holes in an envelope function approxima-

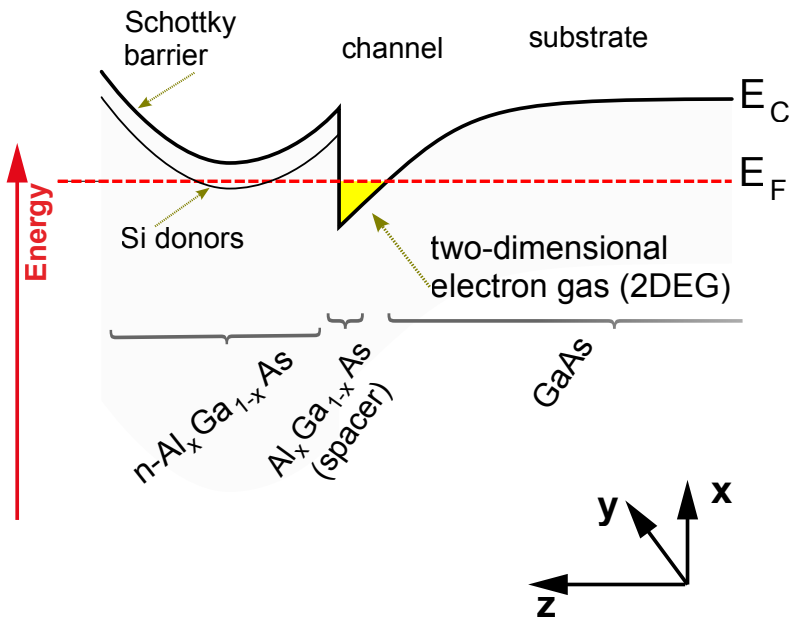

Figure 2.4: An illustration of a band structure of a modulation doped GaAs/AlGaAs heterostructure. Two dimensional electron gas is formed in the triangular quantum well at the GaAs and AlGaAs interface at low temperature.

tion is more complicated compared to electrons in the conduction band. This is because there is a four-fold degeneracy of states; (angular momentum quantum number, $|J, m_j\rangle$) of $|3/2, +3/2\rangle$, $|3/2, +1/2\rangle$, $|3/2, +1/2\rangle$ and $|3/2, -3/2\rangle$ at the top of the valence band. It has been shown that the quantization in the z-direction (perpendicular to the heterointerface) lifts the degeneracy of light and heavy holes resulting in two pairs of degenerate states. The heavy hole degenerate state is at the Γ consisting of $|3/2, +3/2\rangle$ and $|3/2, -3/2\rangle$ states. The heavy hole state are more strongly bound than the light holes at Γ with $|3/2, +1/2\rangle$ and $|3/2, -1/2\rangle$ states. The in-plane dispersion relation for the heavy and light hole quantized states shows that the heavy hole subband has a lighter in-plane mass than the light hole sub-band, resulting in two subband dispersions to cross at finite wave vectors (see fig. 2.5). At the crossing point, heavy and light hole states mix, and results in an avoided crossing. Only the heavy hole subband is occupied in the quantum limit in two-dimensional hole gases.

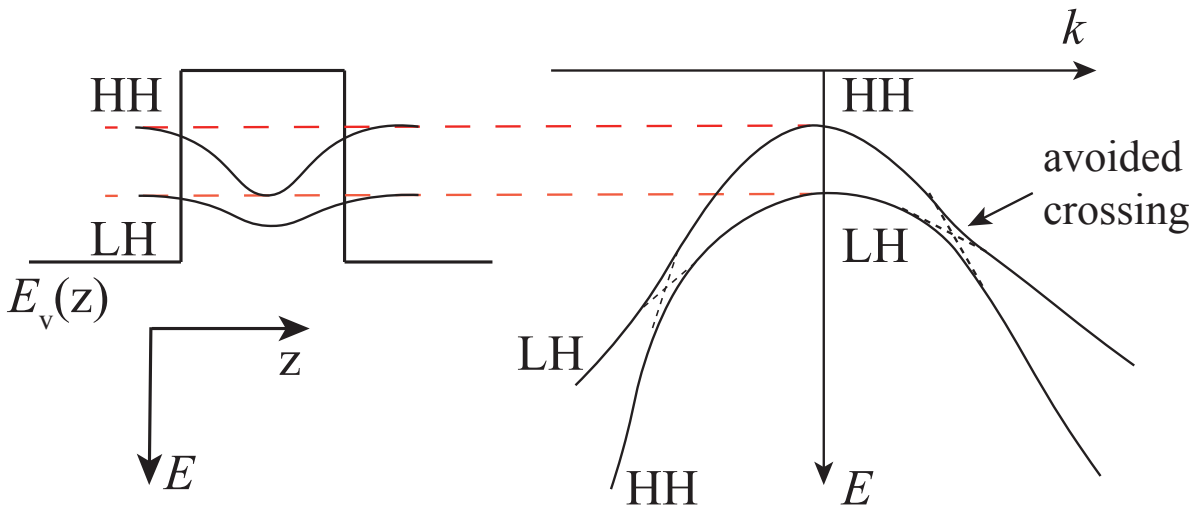

Figure 2.5: Illustration of subband energies and subband states of heavy (HHs) and light holes (LHs) in a quantum well and the dispersion relations of heavy and light holes.

2.4.3 Drude Theory

Drude theory can be used to describe the classical behaviour of electrons in an electric field E. Using Newton's second law, an electron, with charge e, will accelerate in the direction of the electric field, and scatter until reaching a constant velocity, the average drift velocity, v_d, given by

$$v_d = \frac{Ee\tau_t}{m*} \tag{2.11}$$

where τ_t is the mean time between collisions, known as the transport lifetime. We can define the electron mobility as

$$\mu = \frac{v_d}{E} = \frac{e\tau_t}{m*} \tag{2.12}$$

Current density, $\mathbf{J}$, in an electric field is defined as

$$\mathbf{J} = \sigma E = n_e e v_d \tag{2.13}$$

where σ is the conductivity, using above equations the magnitude of the current density

J, j, can be written as,

$$j = n_e e v_d = n_e e \mu E = \frac{e^2 \tau_t n_e}{m*} E \tag{2.14}$$

and the Drude conductivity, σ_D can be defines as:

$$\sigma_D = \frac{e^2 \tau_t n_e}{m*} \tag{2.15}$$

For a constant electron density, σ and μ are limited by τ_t. Thus the average electron velocity at Fermi energy E_f is the Fermi velocity written as:

$$v_f = \frac{\hbar k_f}{m*} \tag{2.16}$$

where k_f is the Fermi wave vector, the mean free path l is

$$l = v_f \tau_t. \tag{2.17}$$

2.4.4 Transport of 2D Electrons in a Magnetic Field

In the classical regime, the general form for the equation of motion of electrons, is given by

$$m^* \frac{dv}{dt} = -\frac{m^* v}{\tau} + q\Big(E + v \times B\Big) \tag{2.18}$$

where τ is the relaxation time between collisions, B is an external magnetic field, v is the velocity of the carrier and q is the charge. When free particles are subject to a magnetic field B, they experience a Lorentz force

$$F = qv \times \mathbf{B} \tag{2.19}$$

As the force is always perpendicular to the direction of travel of the particle, its motion in the absence of other forces is circular, the angular frequency for electrons with charge e can be written as

$$\omega_c = \frac{eB}{m_c} \tag{2.20}$$

where m_c is the cyclotron mass, which is an average over the mass as the electron goes in circular orbits in k-space over a constant energy surface. In the presence of a magnetic field, $\overrightarrow{B}_z$, perpendicular to the travel of electrons, a current density J_x,

flows, the Lorentz force deflects the electrons downwards, resulting in a Hall field, E_H, between the top and the bottom of the surfaces of the Hall bar. The resultant force on the electron $-eE_H$ balances the Lorentz force so the overall drift velocity in the y direction ($\overrightarrow{V_y}$) is zero. Thus the x and y components of the steady state solution for the equation of motion of electrons are

$$E_x = \frac{m * v_x}{e\tau} \tag{2.21}$$

$$E_y = -v_x B. \tag{2.22}$$

To obtain the longitudinal and transverse resistivities, the two results are divided by J_x

$$\rho_{xx} = \frac{1}{n_s e\mu} \tag{2.23}$$

$$\rho_{xy} = \frac{-B}{n_e e} \tag{2.24}$$

As $\rho = 1/\sigma$, the resistivity could be used to determine the electron density, n_e, and mobility, μ.

2.4.4.1 Landau levels

The classical view of electron transport discussed above is only valid for low magnetic fields, $\lesssim 0.5$ T. When the magnetic field is increased the constant density of states, given by equation 2.7, is quantised into Landau levels. Landau levels are the quantisation of the cyclotron orbits of charged particles in a magnetic field. This results in the charged particles being able to only occupy orbits with discrete energy values. The confined electrons move in orbits of quantised radius, r_L, where

$$r_L = \sqrt{\frac{(2n_L + 1)\hbar}{eB_z}} \qquad (n_L = 0, 1, 2, ...) \tag{2.25}$$

where n_L is the Landua level index. However electron motion is unaffected parallel to B_z. The motion of the electrons, in the presence of a magnetic field, can be described by the eigenstates, of the Schrödinger equation:

$$E = \frac{\hbar^2 k_z^2}{2m*} + \left(n_L + \frac{1}{2}\right)\hbar\omega_c \pm \frac{1}{2} g\mu_B B \tag{2.26}$$

where μ_B is the Bohr magneton, g is the Landé g factor and w_c is the cyclotron frequency given by

$$\omega_c = \frac{eB_z}{m*} \tag{2.27}$$

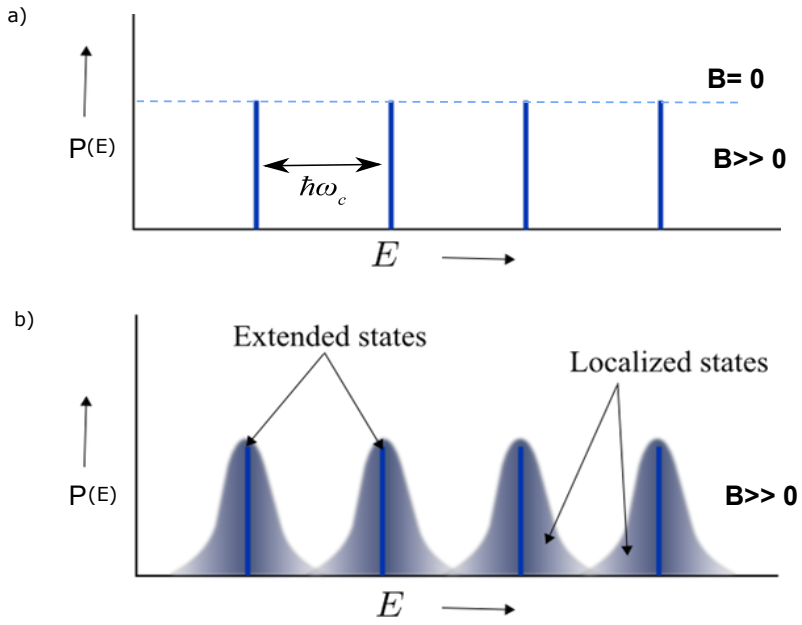

Figure 2.6: *a)* Idealised 2D sample at zero temperature, when a perpendicular magnetic field is applied, the density of states become quantised into non-broadened delta functions, known as Landau levels. *b)* In the presence of disorder such as impurities, and finite temperature, which is present in real 2D samples, the Landau levels are broadened into extended and localised states.

The first term in Eqn. 2.26 is the free electron eigenenergy in the direction of the applied field, and k_z is the wavevector normal to the 2DEG. If only the lowest subband is occupied the first term is fixed due to constant k_z. The third term takes into account spin-splitting effects due to Zeeman splitting. This equation shows that the density of states function in the xy plane is quantised into discrete Landau levels separated by cyclotron energy, $\hbar w_c$. In the presence of disorder, such as impurities and finite temperature present in the real samples, the Landau levels are broadened, into extended and localised states. The observed conductivity is from the contribution of

only the extended states. The total number of populated Landau levels is defined as:

$$\nu = \frac{hn_e}{eB} \tag{2.28}$$

where ν is known as the filling factor. The degeneracy ϱ, in the Landau levels is given by

$$\varrho = \frac{eB}{h} \text{ per spin state} \tag{2.29}$$

2.4.5 Shubnikov-de Haas effect

As the perpendicular magnetic field applied to the 2DEG is increased, the degeneracy of each Landau level also rises, as a result the electrons transfer to lower levels. Provided that the density is unchanged, the Fermi energy E_F oscillates with magnetic field. As the separation between Landau levels increase such that the Fermi energy is within a localised state, the density of the extended states falls to zero, as a result the longitudinal conductivity, σ_{xx} also falls to zero. When the field is increased such that the Fermi energy will be in the extended state of a Landau level, the longitudinal resistivity is low. When E_f is in the middle of the Landau level, the longitudinal conductivity is at maximum. These oscillations are known as the Shubnikov-de Haas (SdH) oscillations, and are periodic in 1/B. The period of oscillation in 1/B is given by:

$$\Delta\left(\frac{1}{B}\right) = \frac{g_s e}{hn_e} \tag{2.30}$$

where g_s is the spin degeneracy. The relationship between longitudinal resistivity and conductivity is given by

$$\rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2 + \sigma_{xy}^2} \tag{2.31}$$

$$\rho_{xy} = \frac{\sigma_{xy}}{\sigma_{xx}^2 + \sigma_{xy}^2} \tag{2.32}$$

Fast Fourier Transform (FFT) of SdH oscillations is a standard analysis technique used on 2DEG [27], and equation 2.30 is used to determine the electron density n_e of 2DEG. The FFT of SdH oscillations can reveal distinct frequencies as a result of spin orbit interaction, intersubband scattering[28], parallel conduction as well as inhomogeneous carrier distribution[29].

2.5 The Quantum Hall effect

The integer quantum Hall effect, first discovered in 1980 by Klaus von Klitzing and his colleagues [5], have stimulated interest in the electrical properties of low-dimensional systems. The quantum Hall effect is observed in 2DEG at low temperatures and strong magnetic fields, where the Hall conductance undergoes quantum Hall transitions, to take on the quantised values. These plateaus coincide with minima in σ_{xx} and occur at resistivities given by,

$$\rho_{xy} = \frac{\nu e^2}{h} \tag{2.33}$$

Due to the high accuracy of the quantisation, this has become the international standard for the definition of the ohm. Using the quantum Hall effect the carrier density and mobility of the 2DEG system can be acquired.

2.6 Electron spin and *g*-factor

The spin S of an electron was introduced by Goudsmit and Uhlenbeck to explain the splitting of spectral lines in a magnetic field. The spin can only have quantised values of S = $\pm 1/2$ for an electron. The spin angular momentum μ_S is given by

$$\mu_S = -g_s \frac{\mu_B}{\hbar} S \tag{2.34}$$

where g_s is the electron spin g-factor, with $g_s \approx 2$. The total magnetic momentum μ is given by

$$\mu = -\frac{g\mu_B}{\hbar} J \tag{2.35}$$

where J is the total angular momentum, $J = |L + S|$, $|L + S|$-1 ,...$-|L + S|$ and g is the Landé g-factor, (from now on will be known as just g-factor), this originates from a combination of the orbital and spin angular momentum, and is given by

$$\begin{aligned} g = g_v \frac{J(J+1) - S(S+1) + L)L + 1}{2J(J+1} + g_s \frac{J(J+1) - S(S+1) + L)L + 1}{2J(J+1} \\ \approx 1 + \frac{J(J+1) - S(S+1) + L)L + 1}{2J(J+1} \text{ where } g_v = 1 \text{ and } g_s = 2 \end{aligned} \tag{2.36}$$

where g_v is the electron orbital g-factor (also known as the valley degeneracy).

2.7 Spin Orbit Interaction

In semiconductors the spin degeneracy of states is the result of spatial inversion symmetry of the crystal lattice and time-reversal symmetry, these together transform the wave vector **k** into **-k**. Time reversal inverts the orientation of the spin, in this case the dispersion relations obey $E_{\uparrow}(\mathbf{k}) = E_{\downarrow}(\mathbf{-k})$, which gives spin degeneracy. This is the case for silicon and germanium. The strength of the spin orbit interaction (SOI), depends on the gradient of the potential and this becomes more important the higher the nuclear charge of the element, with heavy elements showing stronger effects. The SOI in silicon is much weaker than germanium or indium gallium arsenide. The SOI can lift spin degeneracies in the crystal resulting in an effect called spin-orbit split-off band, which is a branch of the valence band lowered energetically due to SOI. In Ge the valence band structure comprises a heavy and a light hole branch degenerate at Γ, and a spin-orbit split-off band that is about $\Delta = 290$ meV lower in energy.

In III-V semiconductors the main sources of SOI, are from structural inversion asymmetry (SIA) [30], arising from the composition and doping differences referred to as Rashba SOI [31]. Another contribution to the SOI appears if the inversion symmetry of the crystal is broken, for example in GaAs, the degeneracy $E_{\uparrow}(\mathbf{k}) = E_{\downarrow}(\mathbf{-k})$ disappears leading to bulk inversion asymmetry (BIA), called the Dresselhaus contribution[32, 33]. Dresselhaus SOI can be engineered in the device design[34, 35], or applied strain controlled during growth[36]. Rashba SOI is dominant in $In_xGa_{1-x}As$ [19, 37] and SIA can be modified with electric fields, enabling gate control of the strength of SOI[37].

2.8 Ballistic Transport in quantum wires

One-dimensional conductance quantisation is one of the most important phenomena displayed by mesoscopic conductors. The quantization can be easily seen in quantum point contact (QPC) structures. A QPC is a nanoscale constriction, connected at both ends of macroscopic reservoirs (see fig. 2.7) with chemical potentials μ_1 and μ_2, through which electrons can travel ballistically at cryogenic temperatures. The connections are assumed to be non-reflecting, and the wire sufficiently narrow so that only the lowest transverse mode in the wire is below the Fermi energy (E_F). As electrons pass through the QPC, the strong lateral confinement experienced by electrons quantises their energy into a series of discrete one-dimensional subbands.

As a simple model based on non-interacting transport that assumes linear response, it is shown that the conductance associated with these subbands takes the universal

value of ($2e^2$/h), independent of the subband index. In 1D the current I is equal to the current density j,

$$j = -ev(\mu_1 - \mu_2)\frac{dn}{d\epsilon} \tag{2.37}$$

where v is the electron velocity and $dn/d\epsilon = 2/hv$ is the density of states in 1D (including the spin degeneracy). As $(\mu_1 - \mu_2) = -eV$, where V is the voltage between the two reservoirs, the conductance (G) is G= I/V =2e^2/h. This derivation is independent of material properties of the conductor or its dimensions making G_0 ($2e^2$/h) a fundamental unit. The ballistic transport is observed at temperatures lower than 4.2 K[38]. QPC's can be created by passing negative current on metallic split-gates on the surface of the semiconductor, which increases the height of the surface Schottky barrier in the region below the surface gates. The bias raises the conduction band energy inside the 2DEG. As a result the width of the 2DEG can be controlled by adjusting the split gate voltage.

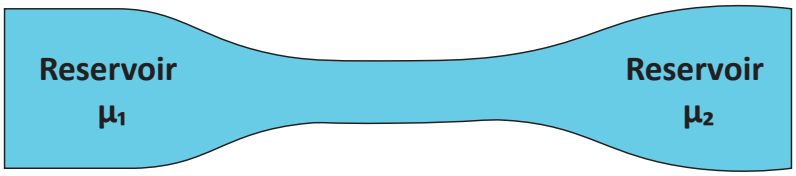

Figure 2.7: Illustration of a one dimensional wire connecting adiabatically two reservoirs with chemical potential μ_1 and μ_2

The 2DEG will eventually deplete to form a 1D constriction, and lateral quantisation of electron energies will occur. Split gates can be used to apply either symmetrical bias to create a 1D constriction midway between the split gates, or differential biasing can be used to alter laterally the position of the quantum wire. This is useful in spin-orbit coupling measurements[39]. Lateral biasing can also be used to 'clean' up the plateau if there is an impurity site causing scattering and creating diffusive transport. Figure 2.8 shows a plot of conductance trough a 1D channel defined in a GaAs 2DEG as a function of split gate voltage. In the figure we can see distinct plateaux, and the inset shows the definition of the 2D channel to 1D.

If the average scattering length is greater than the channel length of the channel, conserving the longitudinal momentum of a propagating electron, then we can observe 1D quantisation. However if the channel length is longer than the scattering length

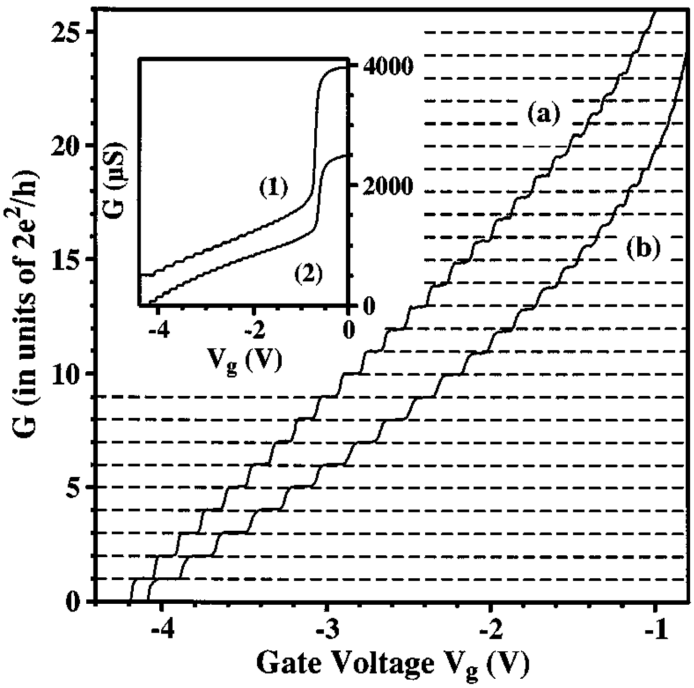

Figure 2.8: Plot of conductance through a 1D channel defined in a GaAs 2DEG as a function of split gate voltage, showing distinct plateaux. The inset shows the complete trace, where the step in the conductance shows the drop in conductance at definition of the 1D channel. (Figure adapted from reference [40])

there will be deviations from quantised conductance. Figure 2.9 shows a comparison of diffusive and ballistic transport.

Electron transport in 1D has been modelled by a number of authors, and mainly relies on the approppiate choice of potential to represent the 1D constriction. While Glazman and Johnson [41, 42] considered a smoothly varying potential at the constriction, Buttiker [43] considered a parabolic saddle point potential in both the x and y plane to represent the constriction. Where the curvature of this saddle point potential (w_x/w_y) affects the clarity of the conductance plateau. This model is adiabatic, where there is no scattering of electrons within the channel. This is known as the Landauer-Buttiker formalism and has become widely accepted to accurately describe the experimental realisation of 1D channels [43, 44, 45].

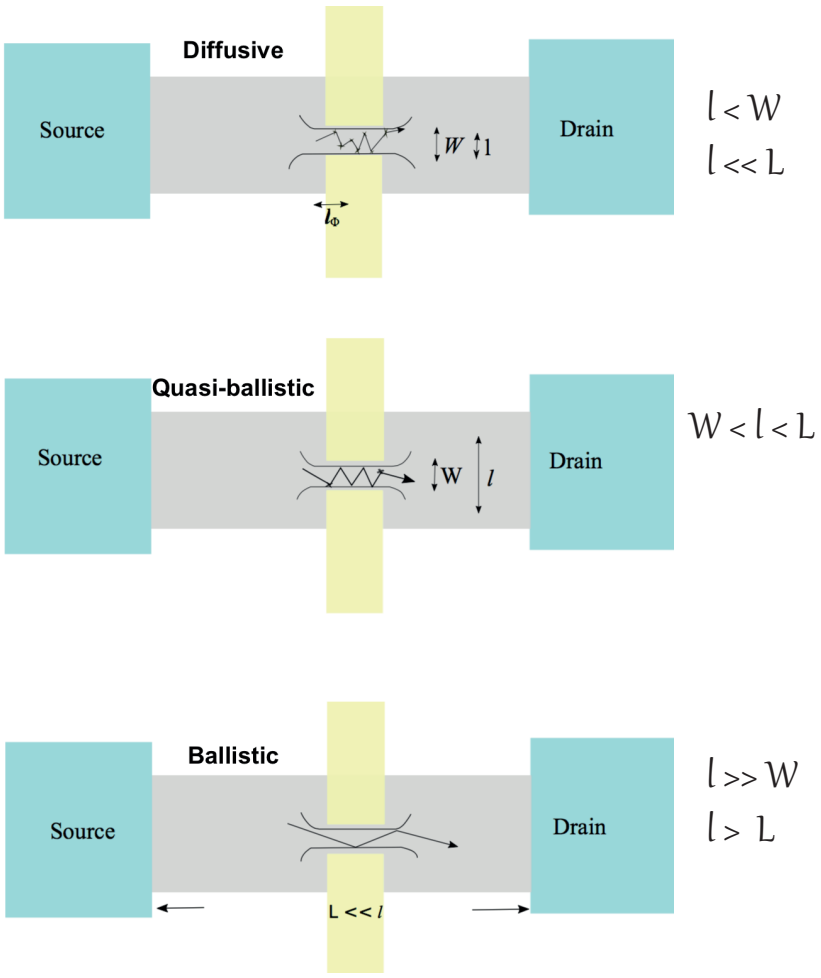

Figure 2.9: Comparison of diffusive and ballistic transport, where L is the length of the wire, l is the scattering length, and W is the wire width.

2.9 $In_{0.75}GaAs$ wafers grown in Cavendish Laboratory

High mobility $In_{0.75}Ga_{0.25}As$ wafers have been successfully grown in the MBE laboratory in the Semiconductor Physics group in Cavendish laboratory. These are still the state of the art $In_{0.75}Ga_{0.25}As$ wafers that are available. Table 2.1 shows the $In_{0.75}Ga_{0.25}As$ wafers that have been grown along with the mobility and densities.

Wafer	Mobility Dark $cm^2V^1s^1$	Mobility light $cm^2V^1s^1$	Density Dark cm^2	Density light cm^2
W402	46830	73500	1.4E+11	3.2E+11
W413	242900	270300	2.3E+11	5E+11
W414	250200	338400	2.2E+11	4.9E+11
W435	264400	424500	2.2E+11	4.4E+11
W436	298400	448000	2.3E+11	4.3E+11

Table 2.1: Table showing the mobility and density of the wafers used in this project. The Mobility and density were determined at 1.6 K.

In this project W402 was used for initial fabrication tests and global top gated devices for magnetotransport measurements and leakage tests for insulators, and W436 was used to study the properties of one dimensional transport and the effects of Rashba spin orbit coupling in 1D transport measurements. Figure 2.10 shows the schematic of the layer structure of W436, which is very similar to all the other wafers listed in table 2.1

2.10 Molecular Beam Epitaxy -MBE

Molecular beam epitaxy is a method of depositing single crystals. Invented at Bell Telephone Laboratories by J.R Arthur and Alfred Y. Cho in the late 1960's [46], MBE has become a widely used method in the semiconductor industry and research institutes. Figure 2.11 shows the schematic of the components in a typical MBE. The growth takes place in ultra-high vacuum (10^{-8} Pa). The deposition rate of MBE is less than 3000 nm/hr. The wafers are grown on a wafer substrate mounted in the UHV chamber, and atoms of different elements are evaporated from quasi-Knudsen effusion cells which are heated until they begin to sublime. The beam of atoms hit the heated substrate, which stick and diffuse around the surface until they find the most energetically favourable place in the crystal lattice. The growth temperatures are around 500°C and 600°C. MBE is used to grow many material combination including Ga, As, Al, Si and In, as long as the influx of atoms, and substrate temperature is appropriate. To grow a

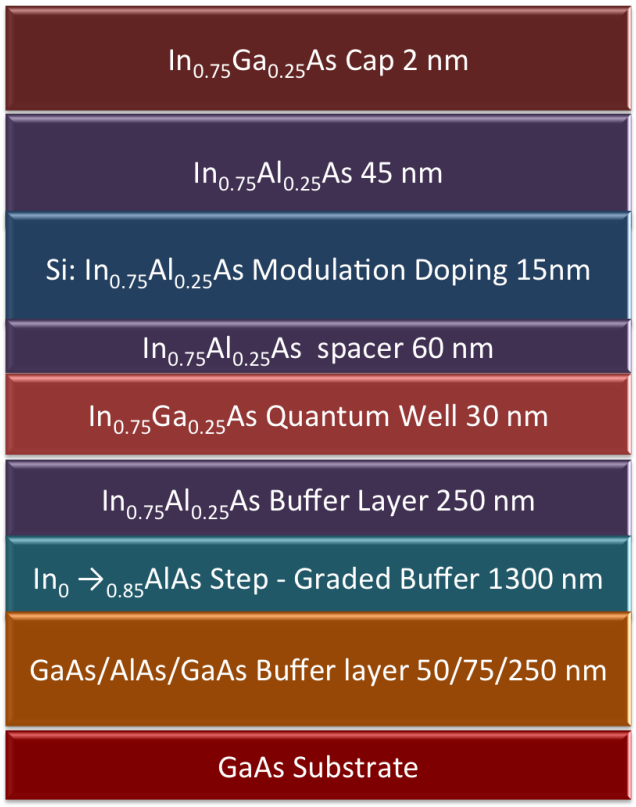

Figure 2.10: Schematic layer structure of W436 with 30nm $In_{0.75}Ga_{0.25}As$ quantum well. Thickness of the layers are not to scale.

certain layer sequence consisting of different materials, their lattice constants have to match in a reasonable manner. GaAs almost matches AlAs, as well as $Al_xGa_{1-x}As$, as a result very high quality wafers can be grown. The interface between these materials have a roughness of less than an atomic layer, as such these layer sequence containing different materials are called heterostructures, and these are an ideal starting point for fabricating complex semiconductor nanostructures.

The thickness of the crystal layers grown is monitored by reflection high energy electron diffraction (RHEED).

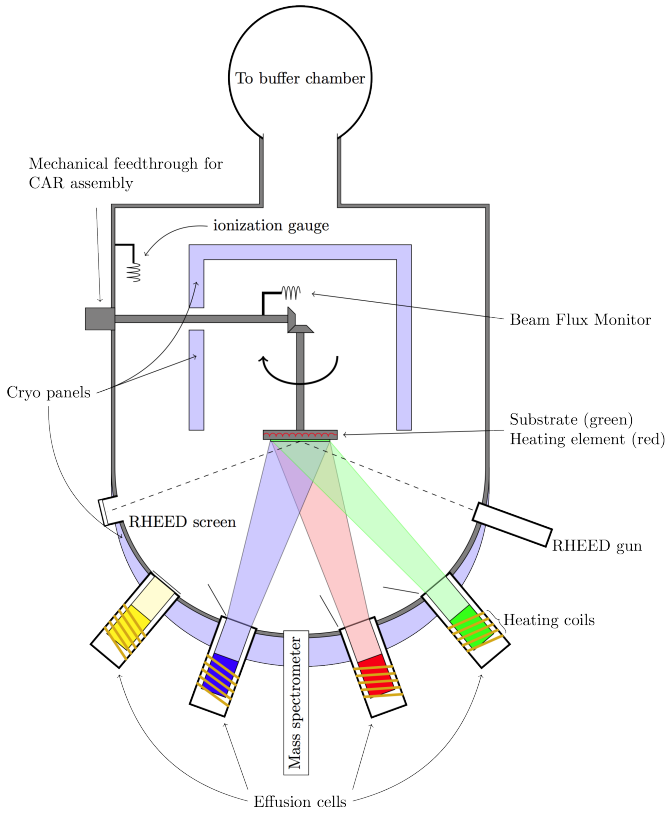

Figure 2.11: Schematic of components in a typical Molecular beam Epitaxy Chamber *("MBE" by "MBE" by Vegar Ottesen).*

2.11 Reduced Pressure Chemical Vapour Deposition (RP-CVD)

The Ge quantum wells were grown using ASM-Epsilon 2000 RP-CVD at university of Warwick. Well established epitaxial growth techniques like solid?source molecular beam epitaxy (MBE), ultra?high vacuum chemical vapour deposition (UHV?CVD) and low?energy plasma?enhanced chemical vapour deposition (LEPE?CVD) are used to grow relaxed Ge buffers on Si. However, in contrast, reduced pressure?chemical vapour deposition (RP?CVD), which is an industrial production technique for modern Si and SiGe device structures, is used to grow the epitaxial strained Ge on SiGe buffer layers. This gives an advantage for scalability for future applications. In reduced pressure chemical vapour deposition, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired material, in this case it is Si and Ge. The by-products produced, are removed by gas flow through the reaction chamber. Reduced pressures in the chamber tend to reduce unwanted gas-phase reactions and improve film uniformity across the wafer.

In the next Chapter the processing methods used to fabricate the devices used in this project along with measurement techniques are described.

Chapter 3

Device Fabrication

3.1 Device Fabrication Methods

InGaAs and p-Ge (2DHG) devices were fabricated in the semiconductor physics laboratory in Cambridge, and the clean room in the London Centre for Nanotechnology (LCN). The majority of the processing were carried out in the semiconductor physics clean room. The sputtering of Nb and e-beam evaporation were carried out at the clean room in LCN.

3.1.1 Cleaving and Cleaning Wafers

The wafers are cleaved into desired size depending on how many Hall bars are required. Typical Hall bar used in this project is 2 mm x 2 mm. Cleaving the wafer requires making short scribes at the end of the wafer to define the chip size, then cleaving by applying pressure to either side of the score, the chip will cleave along the major axis (high mobility direction). Once the desired wafer is cleaved, it is cleaned in an ultrasonic bath in acetone and then propanol for 5 minutes, and dried with N_2. For Ge Wafers a Disco Dicer was used to cut the desired wafer size, as Ge wafers due to the crystal structure is extremely difficult to cleave using a diamond scriber.

3.1.2 Photolithography

Photolithography is an essential method for creating the Hall bars. In this project positive resist was used where the ultra violet (UV) light exposed areas are etched away by the developer. Before each photolithography step the samples were pre-baked on a hot plate at 125 °C to remove any humidity from the samples.

3.1.2.1 Photolithography for Etching

To create a mesa pattern for the Hall bar, Shipley Microposit S1805 resist is spun on to the sample at 5.5 krpm for 45 seconds and post baked for 1 min at 115 °C on a hot plate. The photoresist is passed through a 0.2 μm particle filter and applied to the chip using a glass syringe. After the post bake the mesa pattern (fig. 3.1) is exposed with UV for 3.5 s, and developed using Shipley MF319 developer for 42 s.

The etch solution is usually mixed and left for an hour to stabilise, before patterning. It is prepared by mixing **1:8:120 - $\mathbf{H_2SO_4}$:$\mathbf{H_2O_2}$:$\mathbf{H_2O}$** in a plastic beaker. The wet etch rate for the $In_{0.75}Ga_{0.25}As$ wafers was $\sim$ 6 nm/s. As the quantum well lies about 150 nm deep, it was etched about 180nm. This has worked well for the devices fabricated.

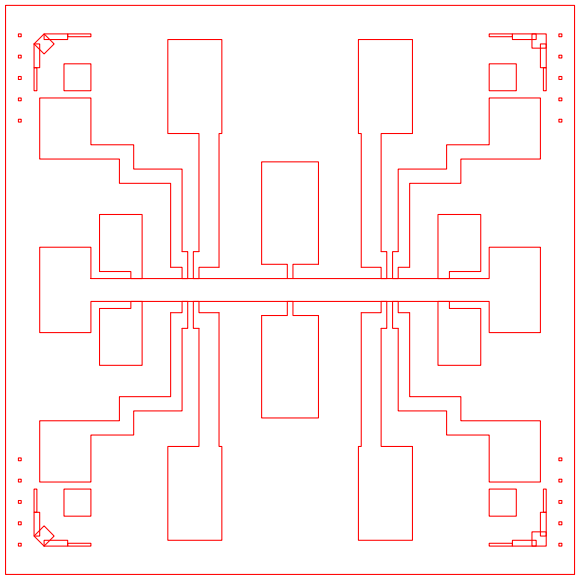

Figure 3.1: The mesa pattern used to create the Hall bar, from the J-11 mask.

Using a Dektak the etch depth was measured. This is a surface contact measurement technique, where a low force stylus is dragged across a surface. First the thickness of the photoresist is measured. Once the required depth is etched, the sample is cleaned in acetone and rinsed in propanol. The sample is then remeasured to obtain the etched thickness without the photoresist.

3.1.2.2 Photolithography for metallisation (Ohmic patterning)

For ohmics patterning Shipley Microposit S1813 is used, this is a thicker photoresist. The sample is heated for 2 minutes at 125 °C to remove humidity and solvents, and the resist is spun at 5.5 krpm for 45 s. The sample is patterned by applying 6.5 s of UV light.

Before developing, the chip is soaked in chlorobenzene for 1.5 min, which hardens the top of the resist for an undercut, this makes sure that the hardened surface is developed more slowly creating an undercut. The sample is then developed in Shipley MF319 developer for 1.5 mins, rinsing in clean DI water, drying with N2.

As Hydrochloric acid etches InGaAs, the sample is put into 40% buffered hydroflouric acid for 10 s to remove oxides which can cause problems for lift off.

3.1.3 Ohmics evaporation and thermal annealing

The ohmic metal used for the samples is a eutectic of Au, Ge, and Ni. Where Au makes the electric contact, and germanium helps to diffuse and dope the surface and nickel helps with adhesion. A tungsten boat is used for the AuGeNi alloy slugs. 500 mg tends to result in 150 nm thickness of metal. The sample is placed in a metal plate that holds the wafer securely facing the source boat. Once the AuGeNi slug and the sample is in place, a bell jar is placed on, and the pump is started, to create a vacuum inside the bell jar. Once the pressure is below 1 x 10^{-6} mbar, current is passed through the boat, which heats up the slug, thermally evaporating the alloy. The rate and thickness is monitored by the quartz crystal monitor. This monitor works by resonating the quartz crystal at a certain frequency, where its frequency of oscillation changes as its mass changes, which is easily calibrated in terms of frequency against deposition thickness for the metal in use. Once the evaporation begins the shutter is opened manually from the side of the evaporator. As nickel evaporates at higher temperature, the current is increased towards the end of the evaporation to get the remaining metal out of the boat. Once the rate is zero, the shutter is closed and the current is slowly decreased.

After the evaporation is complete, the system is kept under vacuum for another twenty minutes for cool down, before taking out the samples. The samples are placed in a jar containing acetone and left for an hour before lift-off. Using a glass pipette, acetone is squirted onto the sample which lifts of the metal, leaving metal only on the exposed places. The lift-off is observed in a petri dish containing IPA, under the microscope to make sure all the metal has been lifted off, and once it is, it is blown dry with N_2. While lifting off the metal, a practice anneal run is activated on the RTP 600S

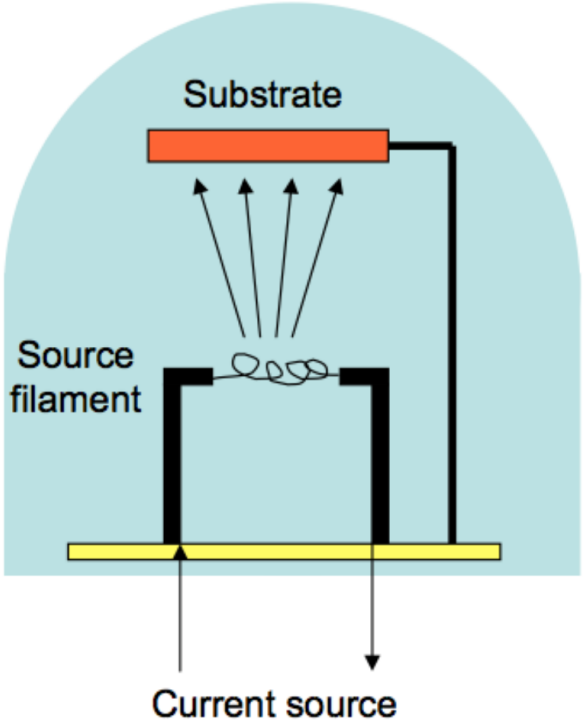

Figure 3.2: Basic illustration of a thermal evaporator.

annealer, to make sure all the parameters that are programmed in run smoothly. The sample is annealed under forming-gas (4% H_2 in N_2) at 430 °C for 80 s. This creates electrical contact with the metal on the surface and the 2DEG, with heavily n-doped columns of Au are formed extending down into the 2DEG. The annealing process is explained in detail in [47] and [48].

3.2 Insulation of Metal Gates

As the Schottky barrier in InGaAs and Ge is suppressed, the metal gates need to be insulated from the surface of these samples for electrostatic operation. SiO_2 was used to insulate the metal gates. About 50 nm of SiO_2 is put on the sample using Plasma Enhanced Chemical Vapour Deposition technique (PECVD). This is a technique widely used to deposit thin films from a gas state to a solid state on a substrate. A plasma is created using an RF (AC) frequency or DC discharge between two electrodes, in which the space in between is filled with the reacting gases. Figure 3.3 shows a basic

illustration of a PECVD.

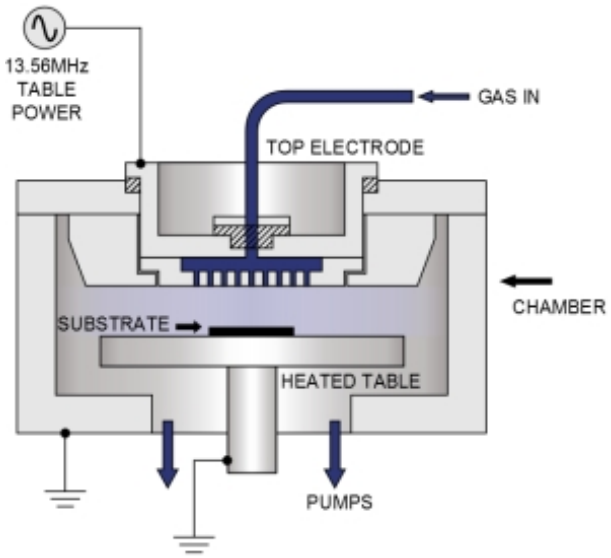

Figure 3.3: Basic illustration of a PECVD, where the substrate sits directly on a heated electrode, the gas is injected into the process chember via the "showerhead" has inlet in the top electrode [49].

The effects of dielectric can be modelled using a capacitor model, where the top gate and the 2DEG are assumed as upper and lower plates, and the SiO_2 is the dielectric, with index i, thickness d_i and a relative permittivity $\epsilon_{r,i}$. the total capacitance C_{Tot} can be written as:

$$\frac{1}{C_{tot}} = \frac{1}{\epsilon_0 A} \sum_i \frac{d_i}{\epsilon_{r,i}} \tag{3.1}$$

where A is the area of overlap between topgate and 2DEG, ϵ_0 is the permittivity of free space. The change in 2DEG density can be determined using the relationship

$$\frac{1}{C_{Tot}} = \frac{V_g}{Q_{tot}} \tag{3.2}$$

where $Q_{tot} = An_{2D}e$, Q_{tot} are the total charge and e is the electron charge. For a given change in gate voltage, ΔV_g and change in 2DEG density Δn_{2D} is given by.

$$\Delta n_{2D} = \frac{\epsilon_0 \Delta V_g}{e \sum_i \frac{d_i}{\epsilon_{r,i}}} \tag{3.3}$$

This model is valid when the 2DEG is fully populated and when there is only a sin-

gle charge carrying layer. The insulating layer can modify the underlying bandgap structure, and sometimes lead to parallel conduction depending on the magnitude of modification of the bandgap of the insulator and conduction band offset [50]. In our devices we have used a thin SiO_2 layer and about 35 nm of di-electiric layer was enough to prevent any parallel conduction on most of the devices fabricated.

After the sample is covered in SiO_2, windows are needed for the ohmic contacts. To open windows, the sample is patterned using positive photolithography technique using the same pattern as the ohmic evaporation but in this case, the sample is immersed in buffered hydrofluoric acid for 30 s, to etch away the SiO_2 on the ohmic windows. To test if it is all etched the sample is probed to see if we can get low resistances between the ohmic contacts.

3.3 Electrostatic Gate Metallisation

3.3.1 RF Ashing

To prepare the samples for e-beam lithography patterning, the sample is cleaned using acetone and IPA, and then to remove any remaining organic compounds, such as photoresist from the sample, RF plasma asher is used, this is also called RF plasma etching. Oxygen RF plasma was used to remove organic matter from the sample. Usually 1 minute of RF plasma was used in the fabrication process.

After RF oxygen plasma, the sample is immersed in 10 % HCl acid for 15 s and rinsed in DI water. The HCl acid removes the oxides on the surface of the sample.

3.3.2 E-beam lithography Preparation and E-beam lithography

The samples are baked in the oven for 10 mins at 150 °C, to remove humidity from the sample.

Two layer PMMA (polymethylmethacrylate), is used for the E-beam lithograhpy. First layer is 100K A6 neat, which has 100,000 molecular weight resins mixed with 6 % anisole. This is spun at 8,000 rpm for 60 s and baked for 3 minutes at 180 °C. Then 950K A11 1:5 MIBK, is spun at 8,000 rpm for 60 s and baked on hotplate for 3 minutes at 180 °C.

The sample is now ready for e-beam lithography. In which the designs are made using Autocad software, and it is possible to write features as small as 10 nm, using e-beam lithography. E-beam lithography works by scanning a focused beam of electrons to draw shapes on a surface covered with PMMA or electron-sensitive resist. The

beam changes the solubility of the regions of the film, enabling selective removal of the exposed or non-exposed regions, when developed.

3.3.3 Surface gate metallisation

For the e-beam defined surface gates, the sample is developed in a mix containing Methyl isobutyl ketone (MIBK), methyl ethyl ketone (MEK) and IPA, 1:5:15, for 8 s, and rinsed in IPA for 15s. Once it is developed, the sample is soaked in 10 % diluted HCl, and rinsed in DI water. Using thermal evaporator 7.5 nm of Ti, and 17.5 nm of Au is evaporated on the sample. The sample is then put into acetone, and after about two hours, the lift off process commences.

For top gated devices, the sample is spun with 950K A4 PMMA, and using e-beam lithography it is crosslinked, to create an insulator on top of the surface gates, before a metal top gate can be put on. This polyamide is transparent at optical wavelengths, and it is a negative resist, and after being exposed by e-beam, it becomes cross-linked and remains on the device after developing. This creates a 100 nm of dielectric on top of the split gates.

3.3.4 Optical gate metallisation

For optical gates defined by optical lithography, the sample is first cleaned using acetone and IPA, then using plasma asher, it is ashed to remove any resist for 1 min, and soaked in 20% HCL for 20 s, and rinsed in DI water and a Weir is used to clean. For optical gates instead of using chlorobenzene for an undercut, LOR is used. LOR is from Microchem, and it is based on polydimethylglutarimide, it is very useful to use as an undercut layer in bi-layer lift-off processing. LOR 7B is spun at 3000 rpm for 50 s and post baked on hot plate for 10 min at 175 °C.

Shipley Microposit 1805 is spun at 3000 r/min for 30 s, baked for 1 min at 115 ° C. The sample is then exposed using J11 Mask (fig 3.4), for 3.5 s and developed in MF319 for 35 s.

Before evaporation the sample is dipped in 20% HCl solution for 20 s and rinsed in DI water.

Thermal evaporator is used to evaporate 20 nm of Ti, and 130 nm of Au. The sample is left to cool in the evaporator for 10 mins after evaporation, and put into SVC-14, a photoresist developer by Shipley, for 10 mins on hot plate at 80 ° C, and a glass pippette is used for lift off.

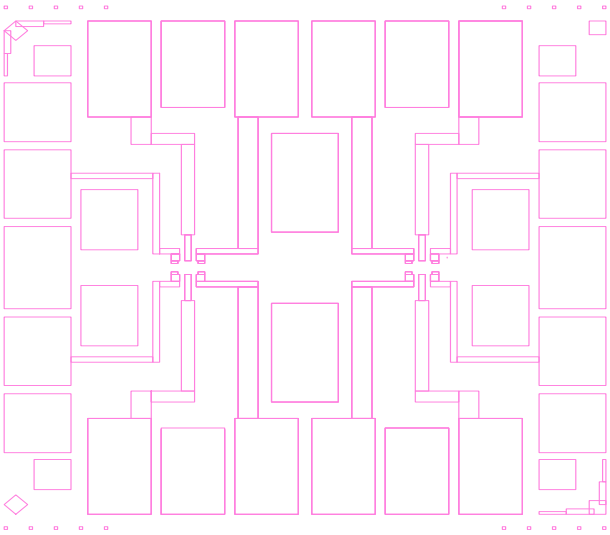

Figure 3.4: J11 Mask for Optical Gates.

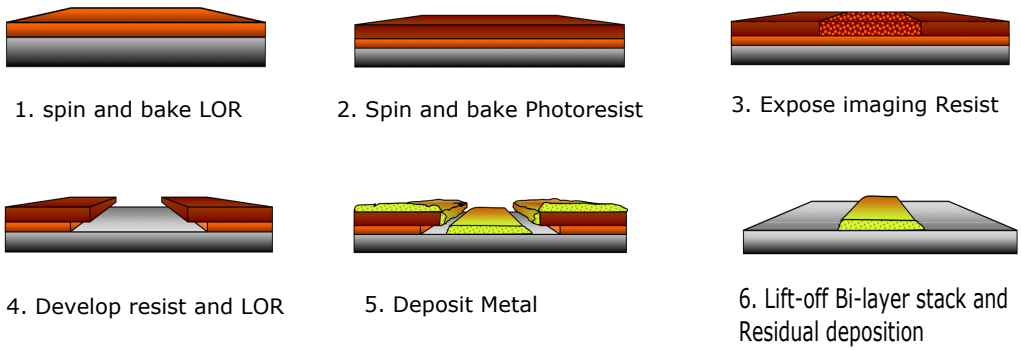

Figure 3.5: Illustration of positive photolithography and lift off after metal deposition.

3.3.5 Packaging

Once the processing is complete, the individual chips are cleaved, using the same technique to cleave the wafer, and glued into non-magnetic 20-pin chip carriers using a GE varnish, and cured at 120 °C. Using a wedge bonder the contacts pads on the device are connected to the chip carrier using Au wire.

3.4 Ge Wafer Processing

The process for fabricating Ge differs slightly. Firstly the ohmic contact material used is aluminium for a p type ohmic contact, and it is annealed at 250 ° for 8 minutes. For etchant we use 1:5:1 ammonium hydroxide:H_2O:hydrogen peroxide. The rest of the processes remain the same as the InGaAs split gate devices. For more details on processing please see Appendix.

3.5 Measurement Techniques and the Cryostats

3.5.1 4.2 K dipping station

Initial measurements were carried out in a liquid ^{4}Helium Dewar, with a base temperature of 4.2 K. Using a simple probe with 24 electrical lines and a red or an infrared LED mounted at the end of the probe, we are able to quickly measure devices, and check if all the contacts work and carry out initial assessment of the ohmic contacts and split gates at the base temperature where the two-dimensional electron/hole gas has already formed.

3.5.2 Four Point Measurement

Four terminal measurement setup was used for the 2D transport measurements. Fig 3.6 shows the circuit arrangement used for four point Hall measurement. An a.c signal of 1 V at a frequency of 33 Hz was provided through a 10 MΩ resistor, to provide a constant current of 100 nA across the device. The device is connected to a lock-in amplifier across a 100 Ω resistor. The voltage across the device is monitored using two separate lock-in amplifiers at the reference frequency of 33 Hz, the setup for longitudinal and horizontal voltage is shown in fig 3.6. The Hall measurements were carried out at the Toshiba Research Labs, using CryoMeas through Acorn computers.

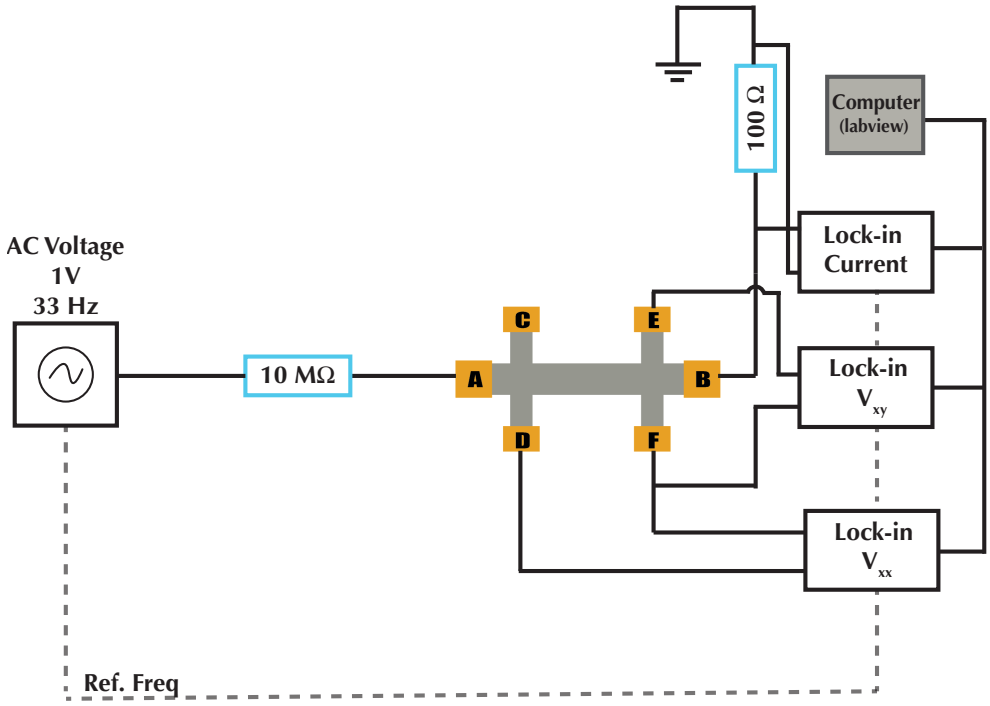

Figure 3.6: Circuit diagram for constant current four-terminal resistance measurements.

3.5.3 1.6 K Measurement for Hall effect and further characterisation

An Oxford Instruments cryostat with a base temperature of 1.6 K at Cambridge Research Laboratory Toshiba (CRL) was used, for further characterisation of devices and for four point Hall measurements. Fig. 3.7 shows a simple schematic of the cryostat used for the measurements at 1.6 K. The cryostat composes of a insulating vacuum jacket with a layer of liquid N_2, which is separated by another layer of insulating vacuum jacket. The inner part of the cryostat is filled with liquid ^{4} He, separating the variable Temperature Insert (VTI), using a needle valve the ^{4}He is introduced to this space in a controlled manner, initially cooling down the sample to 4.2 K. By reducing the pressure below 10 mbar, and controlling the ^{4}He flow rate, the boiling point of ^{4}He is reduced to about 1.5 K, cooling the sample to about 1.6 K and the temperature is kept constant by controlling the flow rate of ^{4}He. The sample sits in a probe in this area with thermal contact to the VTI, and a heater in the sample space can be used to alter the temperature for temperature dependence measurements.

A superconducting magnet that sits in the liquid ^{4}He bath can be used to provide

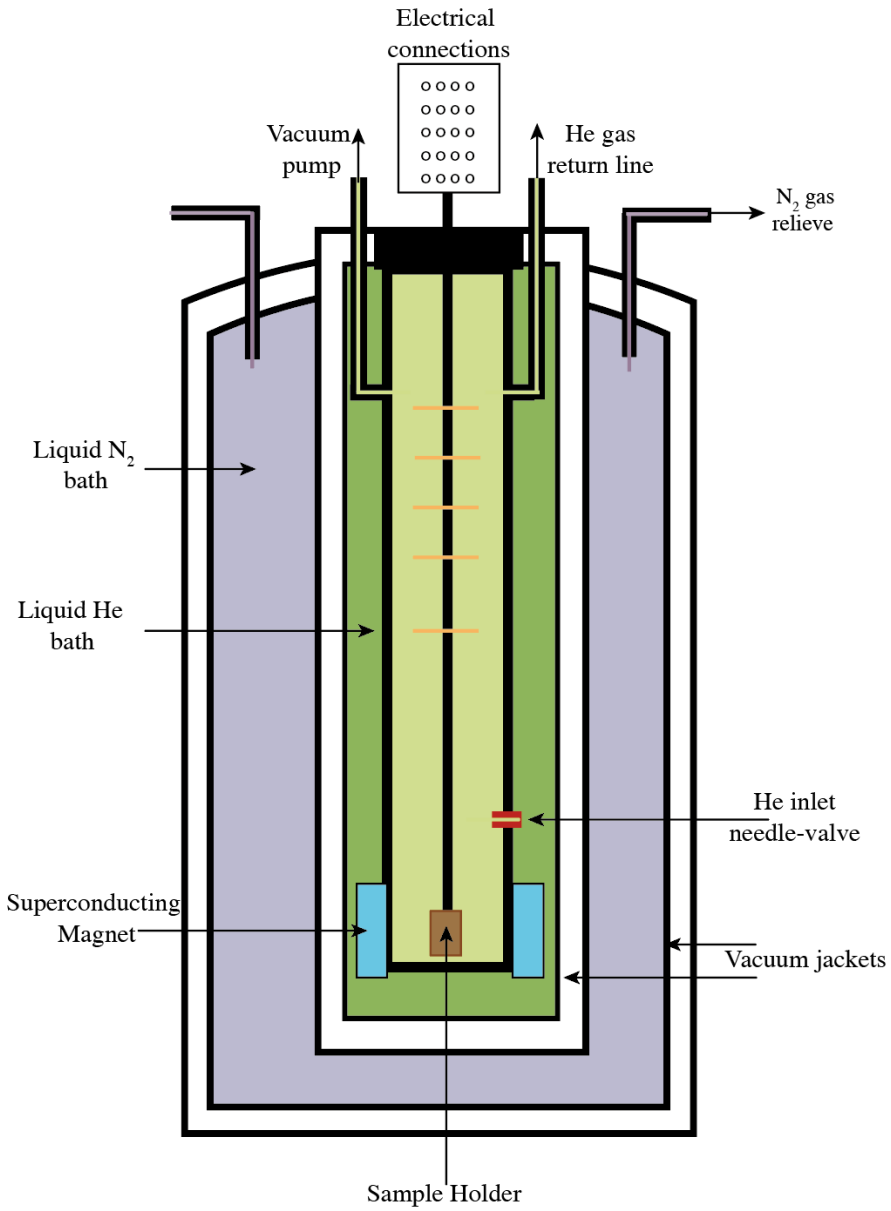

Figure 3.7: Simple schematic of the 1.6K Oxford Instruments cryostat with 10 T superconducting Magnet.

perpendicular or parallel magnetic fields up to ± 10 T, depending on the orientation of the sample.

3.5.4 Heliox system for 350 mK measurements

For measurements below 1.6 K, an Oxford Instruments 'Heliox' system at CRL was used. This is essentially the same system as seen in Fig. 3.7, with a different probe which has a ^{3}He dump. ^{3}He is a light, non-radioactive isotope of helium with two protons and one neutron, hence it has a boiling point of 3.19 K , compared with ^{4}He at 4.2K. ^{3}He is circulated around a closed loop in the cryostat. The sample is attached to the probe and the samples space is kept under vacuum. The probe sits in liquid ^{4}He bath, which cools down the probe to 4.2K. A sorption pump at 4.2 K is used to reduce the pressure above the ^{3}He cooling the sample space to base temperature, until the sorb is saturated with ^{3}He, at this stage it warms up quickly and the sorb should be 're-ignited', this is done by heating the sorb to 45 K to collect the ^{3}He back to the dump. The base temperature stays for about 8 hours in the system used at CRL. This system has superconducting magnets that are able to apply fields up to ± 14 T in perpendicular or in plane.

3.5.5 MX40 system for Measurements at 30 mK

MX40 is from Oxford Instruments, and it is capable to go below 20 mK. This is from 'Kelvinox' series. MX40 is essentially a probe which incorporates the mixing chamber, and all the electrical lines, with a thermal contact to the sample holder. This probe is inserted into a liquid ^{4}He bath, which cools the probe to 4.2 K, and then the VTI is pumped on to reduce the temperature of the 1K pot to about 1.5 K. Once the 1K pot is below 1.5 K, the mixture is introduced to the mixing chamber in parts to start the condensation process, this takes about 6 hours. Once the mixture is fully condensed the mixing chamber temperature can go below 20 mK which is thermally attached to the sample holder. During our measurements the base temperature was between 35 - 50 mK.

3.5.6 Triton 200 system for dry sub 20mK measurement system

Triton 200 is a closed circuit, "dry" dilution cryrostat, that is able to go down below 10 mK. In our measurements we were only able to get a base temperature of 20 mK. This system uses a mixture of ^{3}He and ^{4}He to cool down the sample to the base temperature. Using ^{4}He the top of the stage which sits around 100 K is cooled down to 1.3 K, this is in the outer closed loop. Once 1.3 K is achieved a mixture of ^{3}He and ^{4}He is is introduced to the inner closed loop to cool down further. The inner closed loop is formed of a mixing chamber, a still and a 1 K pot. The mixing chamber is in thermal contact with the sample space. At 870 mK the mixture is separated into two phases, with ^{3}He concentrated phase in the top and a mixture of ^{3}He/^{4}He phase at the bottom. The heat load in the mixing chamber evaporates the ^{3}He first due to its lower mass, as the ^{3}He evaporates, the ^{3}He at the bottom mixture phase starts the break the mixture phase reducing the temperature further, as a result of the relatively large energy to break the mixture phase. The ^{3}He vapour is pumped upwards through the still (600 mK), where the ^{4}He condenses and only ^{3}He passes through. The ^{3}He vapour is then fed through a large vortex tube, with a wide end, where the ^{3}He cools down to become liquid due to sudden change in pressure, and then it is pumped back to the mixing chamber, and this cycles through continously to reach the base temperature and keep it cool for months. The Triton 200 is equipped with 12 T superconducting magnets to provide perpendicular/in-plane magnetic field.

Triton 200 has a bottom loading system, and it takes about 8 hours to get to base temperature from room temperature, see figure 3.8.

Figure 3.8: Image of the Oxford Instruments Triton 200 dilution cryostat at London Centre for Nanotechnology.

3.6 Series Resistance Correction

In a two terminal measurement system, the measured signal must be corrected for series resistance caused by the connections, the resistors in the filters and the resistance caused by the ohmic contacts. Removing the series resistance increases the accuracy of the measurement. To correct for the series resistance we assume that in the open-channel where the split gate voltages $V_{sg} = 0$, $R_{device} = 0$ therefore the series resistance R_s is 1/G at V_{sg} =0. The conductance with series resistance removed is:

$$\begin{aligned} G &= \frac{i_m}{V_m - i_m R_s} \\ &= \frac{1}{(\frac{V_m}{i_m} - R_s)} \\ &= \frac{1}{(\frac{1}{G_m} - R_s)} \end{aligned} \tag{3.4}$$

where i_m is the measured current, V_m is the applied voltage and G_m is the measured conductance. The conductance in the 1D channel in units of $2e^2/h$ is given by

$$G\left(\frac{2e^2}{h}\right) = \frac{1}{\left((\frac{1}{G_m}) - R_s\right)} \frac{1}{77.3 \times 10^{-6}} \tag{3.5}$$

Subtracting the series resistance from the differential conductance will correct the conductance plateaus, and the quantised conductance plateaus will align to their quantised values.

Chapter 4

Previous Work on InGaAs and Characterisation of InGaAs

4.1 Wafers grown at the Cavendish laboratory

GaAs/AlGaAs modulation-doped heterostructures have been grown extensively for the last 40 years, and ultra high mobility wafers have been demonstrated [26] thanks to various improvements in the design of MBE chambers and device heterostructures [51]. The ternary compounds $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ are compounds of interest due to their properties, such as high effective g-factors [52], lower effective mass of electrons [20], resulting in high peak electron velocities for a given field electron density, high low-field electron mobilities and increased electron subband energy spacing [21]. Although the QWs confined in InGaAs/InAlAs have the potential to have higher electron mobilities than 2DEG confined in GaAs/AlGaAs due to the smaller effective mass of the electrons, it has not been possible to achieve mobilities above 4.4×10^5 $cm^2V^{-1}s^{-1}$. The main reason arises from scattering due to alloy disorder in InGaAs [53]. Scattering from background impurities is also a limiting factor [53, 54, 55, 56].

As shown in figure 4.1, the absence of lattice matched substrate for growing $In_{0.75}Ga_{0.25}As$ introduces high strain into the epitaxial layer, resulting in formations of dislocations, leading to deterioration of the crystal quality and carrier mobility. This led to the development of graded InGaAs/InAlAs layers to be grown on GaAs substrate [58], exhibiting very low dislocation densities.

The $In_{0.75}Ga_{0.25}As$ QWs studied in this project were grown by solid-source MBE using a Veeco Gen III system on 3 inch semi-insulating (001) GaAs substrates. A schematic of the layer structure grown is shown in figure 2.10.

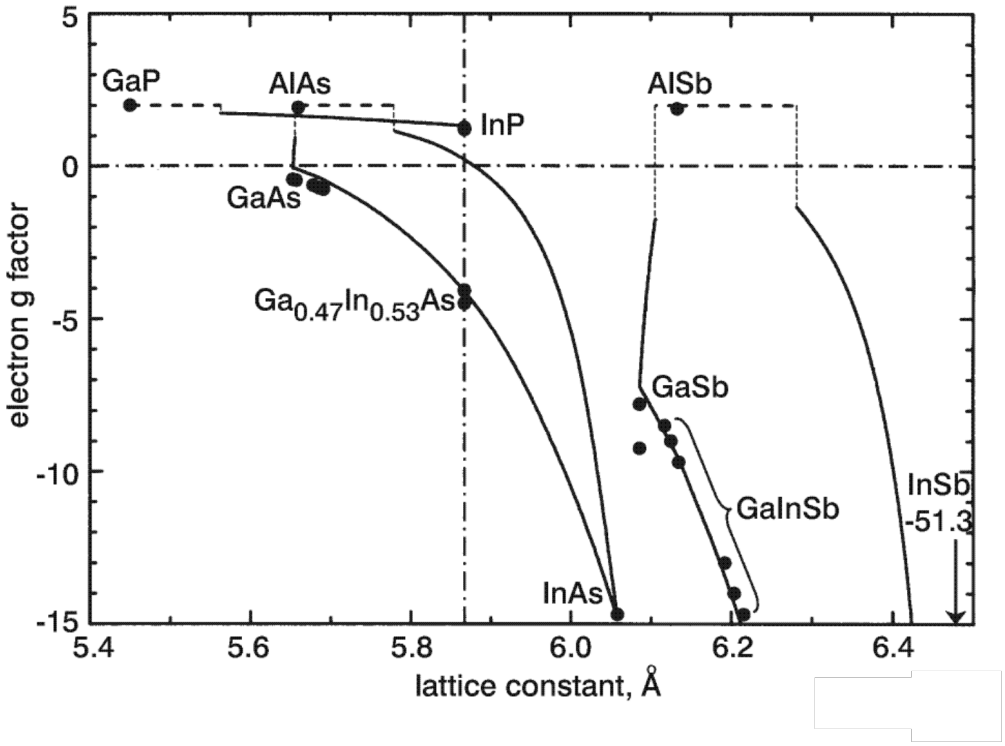

Figure 4.1: The g factors for conduction band electrons in III-V semiconductors as a function of lattice constant [57].

4.1.1 W402 wafer and characterisation

The W402 wafer has been mainly used as a test wafer, as it has the same layer structure as W436 (see fig.2.10). In order to preserve material from the high mobility wafers, we have been using W402 to optimise our processing methods and find a suitable dielectric to prevent leakage currents. Previous Toshiba case student Mark Fletcher has tried out several dielectrics on InGaAs, and SiO_2 was found to be sufficient, his proposal to use AlO_3 using atomic layer deposition method to achieve thinner dielectric was not tested. In this project SiO_2 was sufficient and no leakage, or parallel conduction problems arose.

Since the 2DEG measurements on the wafers used in this project have been extensively studied by Dr Chong Chen and Dr Stuart Holmes, Hall measurements were only carried out on W402 wafer simply to test the fabrication methods, and make sure that the SiO_2 insulating layer was sufficient for having leakage free devices. Once the fabrication method was deemed successful, we made the first split gates using W402, and when this worked we have moved on to make split gates on W436 wafer, which has

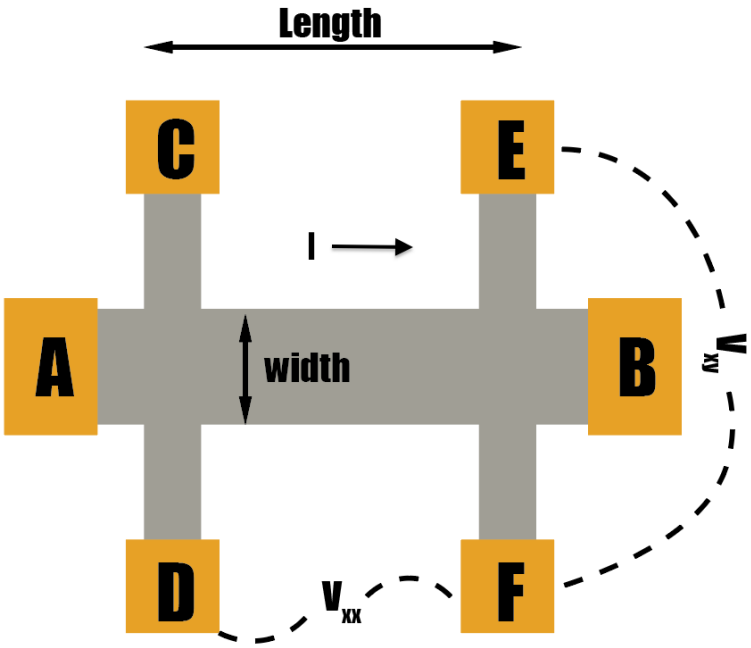

Figure 4.2: Four terminal measurement setup for a Hall Bar used in the experiment. Current is passed between contacts A-B. Vxx is measured between contacts D-F and C-E. Hall voltage, Vxy, is measured between contacts C-D and E-F.

the highest mobility out of the wafers that are currently available.

W402 wafer has a mobility of 4.7 $\times 10^4$ in dark, 7.4 $\times 10^4$ cm$^2 V^1 s^1$ in light with density of 1.4 to 3.2 $\times 10^{11} cm^2$ in dark and light respectively. Hall Measurements were carried out at 1.6 K at Toshiba 10 T cryostat. From the measurements the mobility and carrier density were determined. Figure 4.2 shows the four terminal measurement arrangement for the Hall bar geometry. The magnetotransport measurements were performed, using constant current mode (100 nA), with standard lock-in technique. The Hall effect was used to measure the two dimensional carrier density n_{2D}, along with Shubnikov-de Haas oscillations. Figure 4.3 shows the longitudinal, (R_{XX}) , and transverse (R_{XY}), magnetoresistances on the W402 Hall bar, at different top gate voltages, to establish mobility as a function of electron density. In the figure we can see that the Hall slope is straight and quantised Hall-plateaux are flat at both at -0.3 V on top gate and 0 V on top gate, confirming that there is no parallel conduction.

Table 4.1 summarises the results from the magneto transport measurements.

$\mathbf{V_g}$ **(V)**	$\mathbf{R_H}$ **(Ohm/T)**	$\mathbf{N_H}$ **(cm^{-2})**	$\mathbf{N_{SDH}}$**(cm^{-2})**	ρ_0**(Ohm/SQR)**	μ**(cm^2/V.s)**
0	2516	2.48 x 10^{11}	2.4 x 10^{11}	493	51000
-0.3	3162	1.97 x 10^{11}	1.9 x 10^{11}	712	44400

Table 4.1: Summary of the results from the Hall measurements.

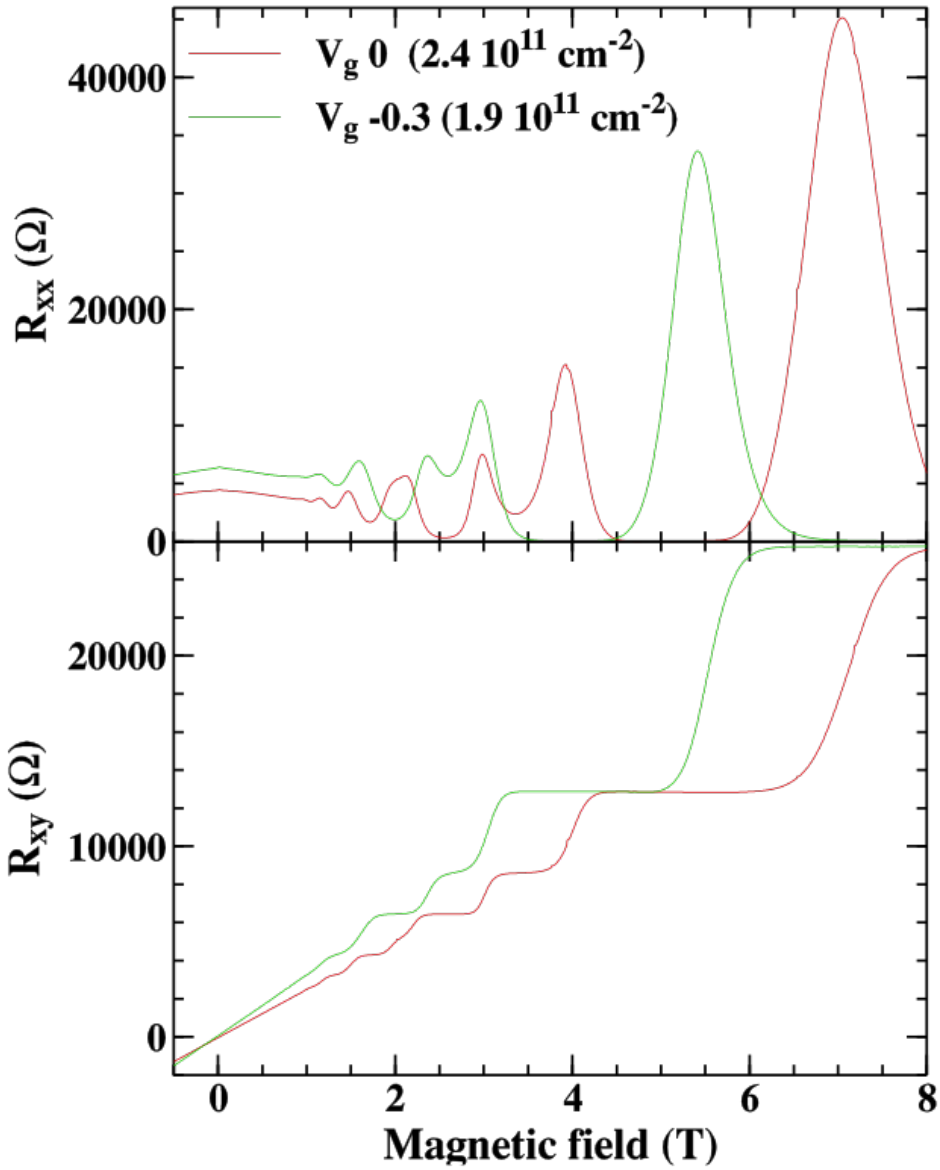

Figure 4.3: Longitudinal (R_{XX}), and transverse (R_{XY}), magnetoresistances on the W402 Hall bar, at different top gate voltages.

4.2 Split gates on W402

E-beam defined split gates were fabricated using W402, the length of these split gates varied from L = 700 nm to 1 μm and width ranging from W= 400 nm to 1 μm. Initial tests were carried out at the 4.2 K dip station. Figure 4.4 shows the split gate data at 4.2 K. At this temperature we do not expect to see fully ballistic transport, but it is a quick way to establish if the gates deplete the channel, and if the ohmic contacts are working. In the figure we can see the curved region just below 0V this is the definition region where the gate defines the 1D region as the negative voltage is increased (see inset to fig. 4.5).

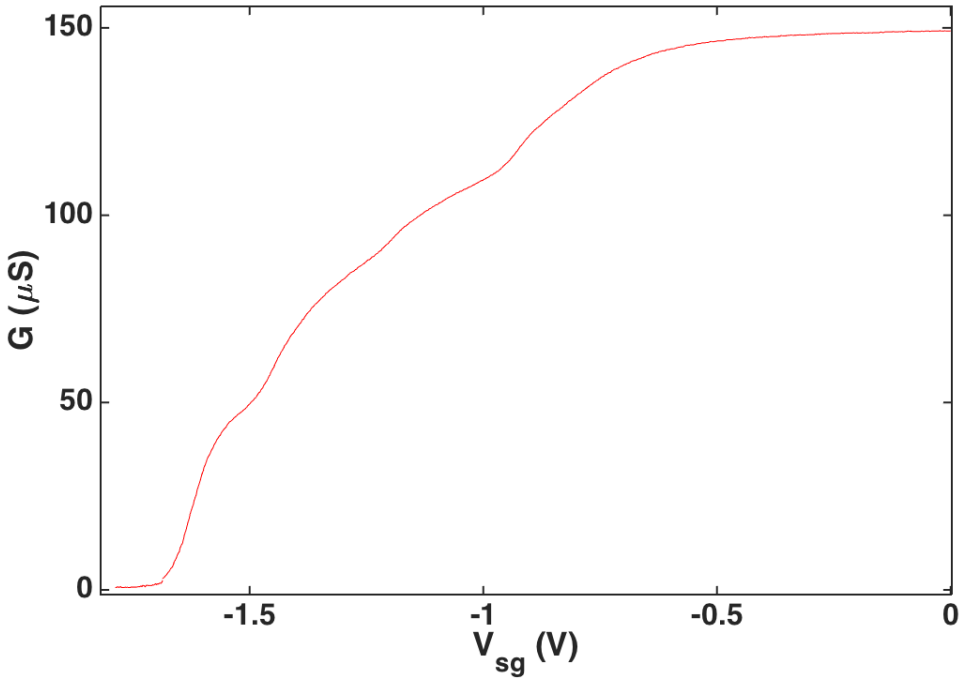

Figure 4.4: Differential conductance as a function of split gate voltage for the split gates on W402 at 4.2 K.

Having established that the gates are working in the dip station, the split gates were measured at 1.6 K at Toshiba. Figure 4.5 show the conductance data at 1.6 K using 50 μV excitation voltage. Using symmetric negative gate-bias (V_{sg}) a 1D channel in the 2DEG is created midway between the split gates. First measurements were made in the dark and negative voltage was applied to the split gates until the channel was

depleted. In the figure we can see plateaux at 2 and $3(2e^2/h)$, but there is no plateau at $2e^2/h$ and there are structures near the depletion, indicating that there are a lot of impurity sites and the channel is quasi ballistic. The figure also shows conductance data after illumination, in this instance the illumination had minimal effect on the transport properties in the channel, though pinch-off voltage have increased due to higher carrier density, but the channel is still quasi ballistic.

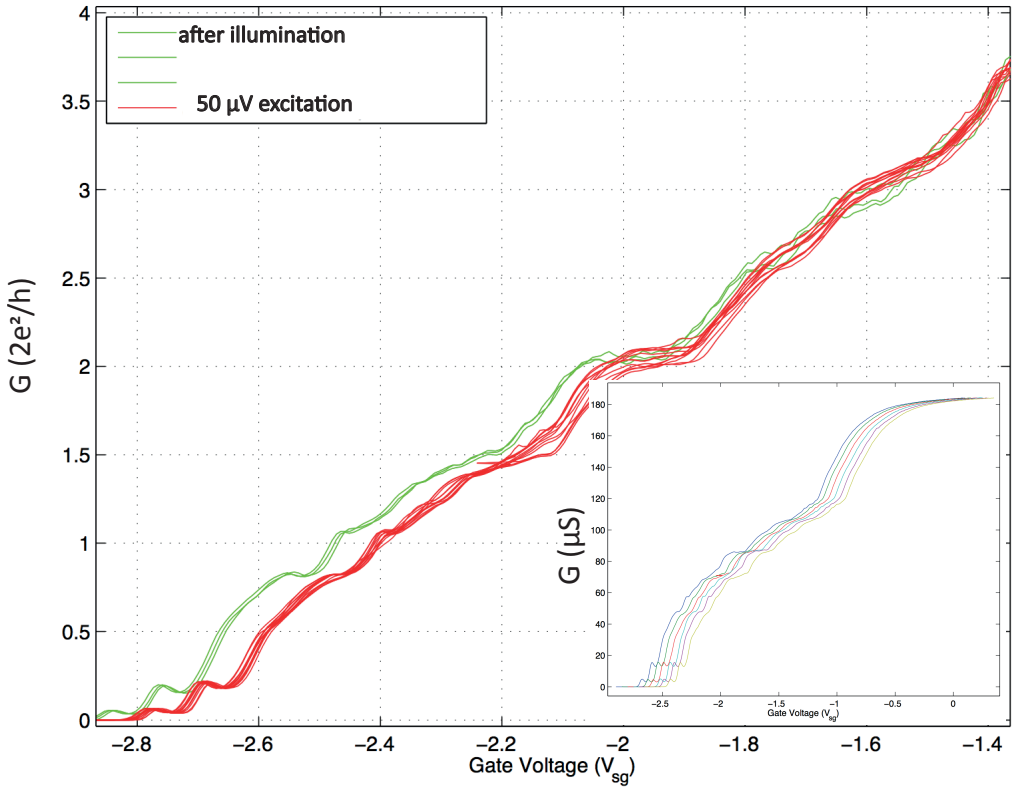

Figure 4.5: Differential conductance as a function of split gate voltage on W402 at 1.6 K. Data has been corrected for series resistance. Inset conduction data without R_{series} removed before illumination as a function of gate voltage.

4.3 First split gates on W436

First split gates made on W436 had a length ranging from 200 nm to 500 nm and a width ranging 500 nm to 1 μm. Ballistic transport in semiconductor nanowires plays a central role for possible applications in quantum logic devices [59]. In order to observe

quantisation the width of the channel must be comparable to the Fermi wavelength of the electrons, and the temperature must be low compared to the characteristic energy spacing of transverse modes in the channel. It is important to get the geometrical parameters right in order to observe defect-free ballistic transport. The electron mean free path of the W436 wafer is 2.3 μm at a electron density of 2.3 x 10^{11} cm^{-2} so split gate lengths should be below this value. There are various factors that can effect ballistic transport in gate defined quantum wires, as the optimal design to achieve good electron confinement was unknown, the most effective way was to start with different sized split gates. Using J-Mask 11 (see fig 3.1) allowed us to have 6 different split gates on to a single Hall bar. Table 4.2 summarises the gate sizes used for the initial gates made on W436.

Split Gate	Length (nm)	Width (nm)
1	200	500
2	200	700
3	400	500
4	400	700
5	400	1000
6	500	700

Table 4.2: The sizes of the first set of split gated devices on W436

Background impurities lead to quasi ballistic transport. The background impurity density in wafer W436 is 5 x $10^{15}cm^{-3}$, which results in the impurity spacing to be $\approx$ 60 nm. Therefore narrow gates are needed to avoid quasi ballistic transport due to scattering. The split gates were initially measured at 4.2 K. Figure 4.6 shows the conductance data for the split gates with 200 nm length and 700 nm width measured at 4.2 K. In the figure we can see that the 1D channel is defined at -1.2 V. We can also see additional plateau like features, but as the temperature is high we do not expect to see clear quantised conductance at this temperature. Additional 1D transport measurements can be carried out at 4.2 K, such as d.c. source drain measurements, to see the ballistic nature of the channel. Figure 4.7 shows the d.c bias spectroscopy applied up to 10 mV at 4.2 K. In the figure we can clearly see the 0.25 G_0 structure, which confirms the ballistic nature of the channel [60]. The 0.25 G_0 arises from momentum degeneracy being lifted by d.c source drain bias and the channel becomes fully spin polarised. Looking at the data from 4.2 K, we have decided to measure this device at lower temperature, and further measurements were carried out at 50 mK using the MX40 at the Cavendish Laboratory.

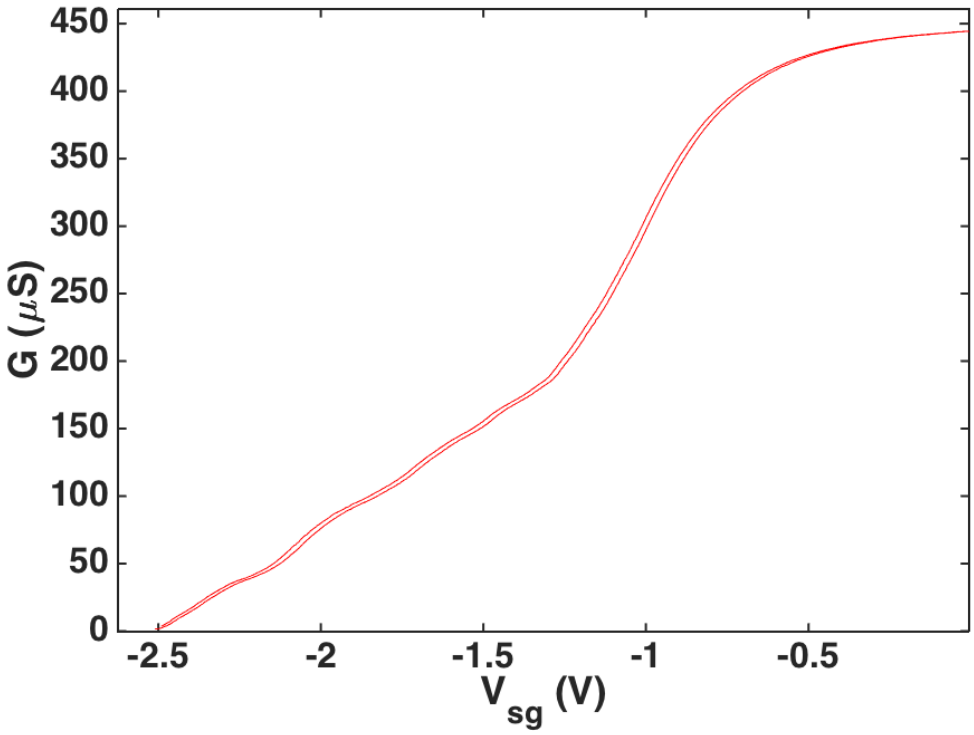

Figure 4.6: Differential conductance as a function of split gate voltage for the first split gates on W436 measured at 4.2K.

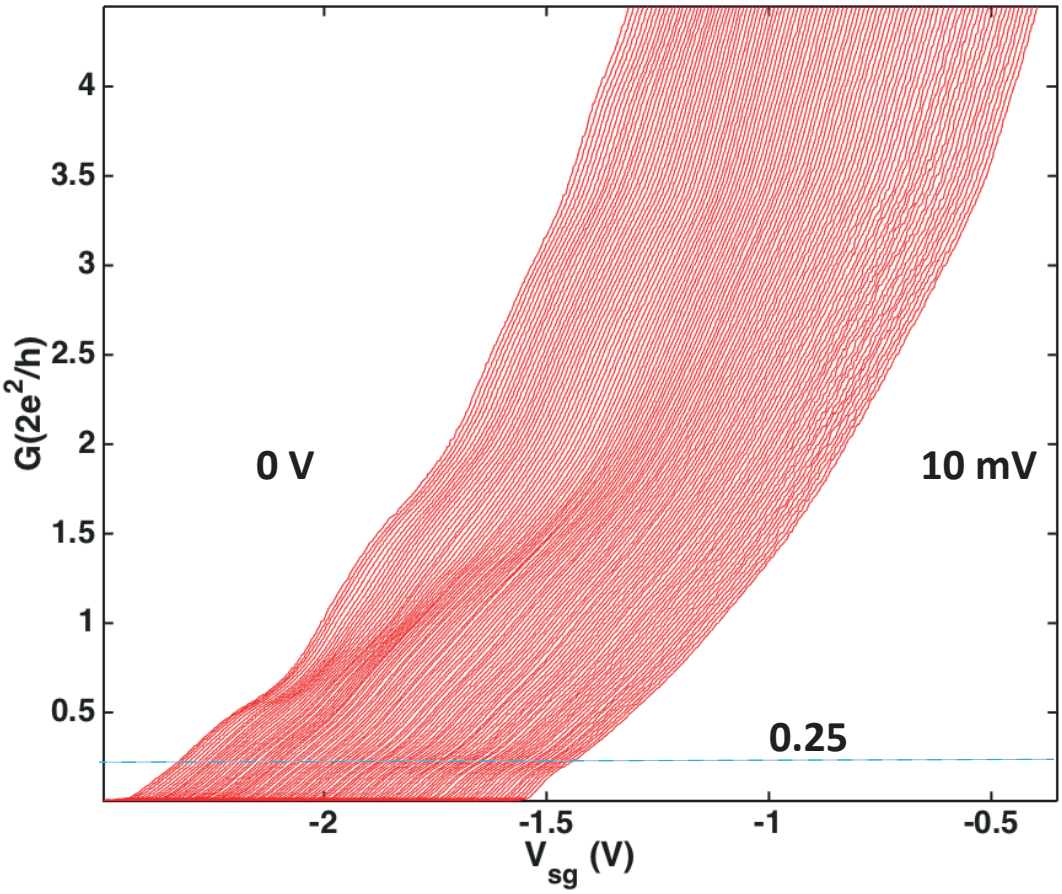

Figure 4.7: d.c bias spectroscopy from 0 V to 10 mV. Data has been offset horizontally for clarity.

4.3.1 Low Temperature Measurements

At lower temperatures Universal Conductance Fluctuations (UCF) can be a problem. This was the observed case for the first split gates measured on W436 at 35 mK using the MX40 fridge. UCF's arise from coherence effects for electronic wavefunctions. To avoid UCF's the phase-coherence length l_ϕ needs to be larger than the momentum relaxation [61] length l_m. Figure 4.8 shows the conductance data for the first cool down of the split gate. A 100 μV of excitation voltage was applied through the source and drain, and the split gates were swept from 0 V until depletion using a symmetric negative gate-bias (V_{sg}). As the temperature is reduced we see UCF like structures along with coulomb blockade structures near the pinch off [7]. There are various methods to reduce this, such as applying small perpendicular magnetic field to reduce backscattering from impurities close to the quantum wire [38, 62]. The fluctuations can also be reduced by illuminating the device in order to increase the mobility and carrier density hence increasing the electron mean free path. The electron mean free path after illumination is 2.3 μm. Although we would expect ballistic transport with the dimensions of the split gates, other factors such as impurity sites can affect the ballistic transport. Figure 4.9 shows the same device after illumination, and from the figure we can see that most of the UCF like structures have disappeared. However the plateaux although visible are not very clear.

4.4 Summary

In this chapter, the initial measurements carried out on W402 and W436 were summarised. These measurements were useful to determine the ideal length scales that were needed to get clear quantised conductance, and it has also helped us to determine the fabrication methods needed to produce high yield working devices. We have made further devices using the same wafer, including top gated devices. We have also made further devices with a mid line gate, and narrow split gates. The following chapter summarises the measurements made using the narrow split gates, and further measurements carried out to determine the g factor, and the effects of Rashba spin orbit coupling.

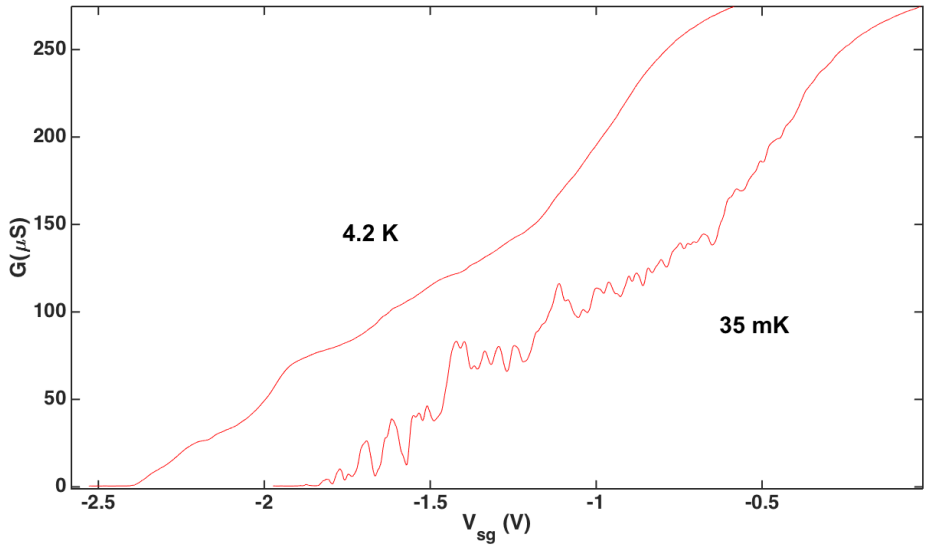

Figure 4.8: Differential conductance as a function of split gate voltage at 4.2 K and 35 mK. The length of the split gate was 700 nm and the width was 1 μm. Data has been offset horizontally for clarity.

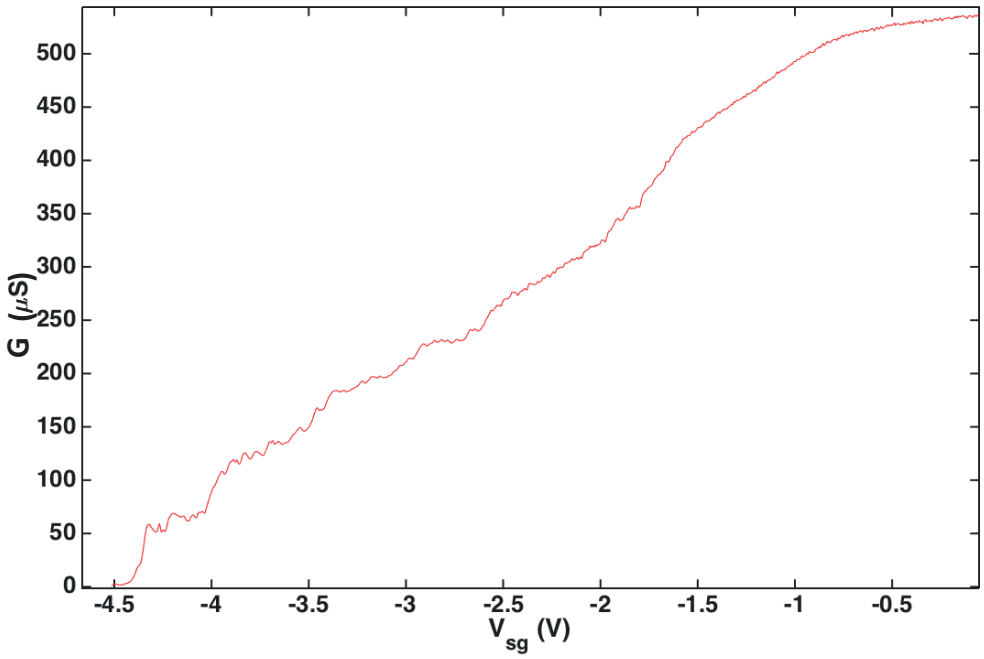

Figure 4.9: Differential conductance as a function of split gate voltage after illumination. R_{series} not removed.

Chapter 5

1D Transport Measurements on high mobility $In_{0.75}Ga_{0.25}As$ Quantum Point Contact (QPC) devices

5.1 Introduction

Chapter 4 summarised the early work carried out on the lower mobility wafers and initial transport measurements carried out using the high mobility W436 wafer. These measurements have helped us to determine an ideal length scale for the next set of devices. This chapter summarises the low temperature transport measurements carried out on narrow split gated devices on W436. We also determine the g factor using the method developed by Patel *et al.* [63].

Previous studies on InGaAs quantum wells have revealed interface scattering to be the limiting mechanism for electron transport [64]. It was found that low mobility devices exhibit large number of UCFs in the measurements and ballistic transport was not observed (see chapter 4), but as the mobility increased we see that scattering, most likely due to alloy disorder reduce significantly and quantised conductance can be easily seen without applied external magnetic fields. Alloy disorder occurs mainly in ternary compounds such as $Al_xGa_{1-x}As$, as ions with different sizes in the crystal lattice cause a loss in periodicity, resulting in electrons experiencing a randomly spatially varying potential [65, 66]. Scattering lengths and electron mean free path also effect ballistic

transport. The narrow split gate devices measured here show quantised conductance similar to GaAs devices. Although there is still noise due to alloy disorder and scattering through impurities which is visible in the measurements.

5.2 Device parameters and measurement circuit

1D electrical transport measurements were performed on narrow gates fabricated on W436 wafer following the procedure outlined in section 3.1, one of the device fabricated was a double quantum dot design with a narrow middle gate that can act as a split gate (Device A fig. 5.1) when the dots are not defined. This device has a length of 40 nm and a width of 100 nm. Further measurements were carried out on another split gate with a wider channel (Device B). This device showed near defect-free ballistic conductance, this device has a length of 200 nm and a width of 400 nm. The metal gates are insulated from the surface of $In_{0.75}Ga_{0.25}As$ by 50 nm of SiO_x. The SiO_x was deposited using PECVD, which produce conformal deposition over simple surface profiles such as mesa side walls, giving uniform thickness across the surface. Figure 5.2 shows an SEM image of the device A used in the experiment, along with the measurement circuit. The surface gates were patterned using e-beam lithography, and Ti/Au was used for the gate contacts.

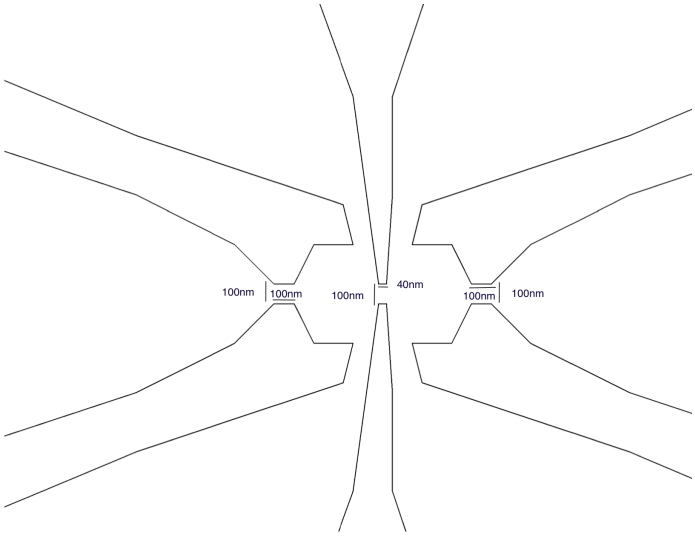

Figure 5.1: Schematic of device A with dimensions.

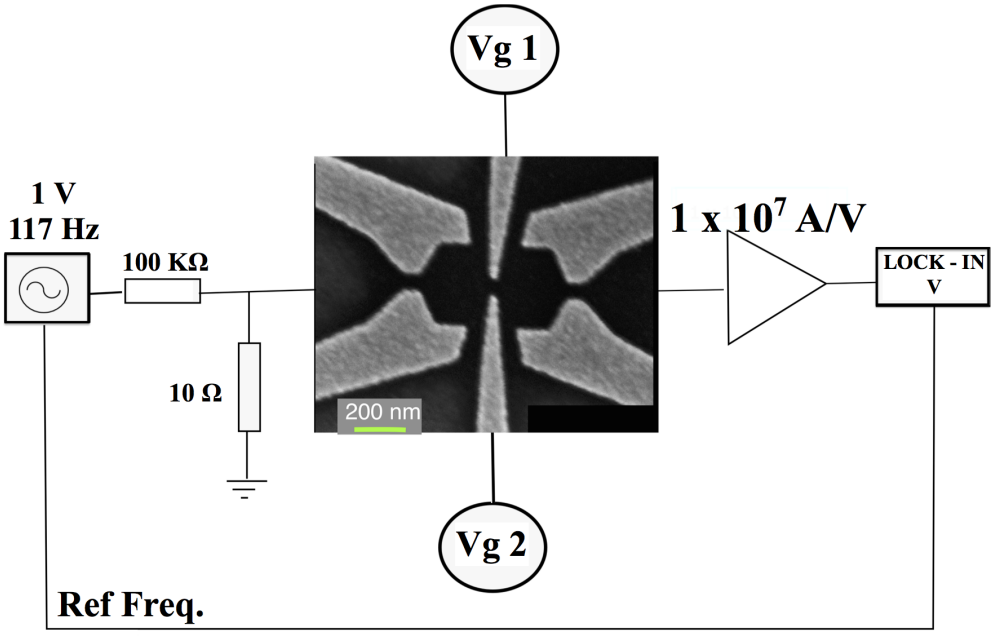

Figure 5.2: Measurement Circuit used in the measurement, with SEM image of device A.

5.3 Device Characterisation

The devices were measured using an Oxford Instruments Kelvinox MX40 dilution fridge, with a base temperature of 30 mK, during the measurements of Device A the base temperature was around 38 mK, and 50 mK during the measurement of device B. Both sides of the split gate were symmetrically swept from 0 V to negative V until depletion and swept back to 0 V during cool down using a DAC voltage source. An a.c signal of 1 V, at a frequency of around 77 Hz was applied via a potential divider, reducing the signal to the device. This is done by using a 100 kΩ resistor in series between the signal generator and the device, with a second 10 Ω resistor connected to the ground. This resulted in 100 μV a.c voltage across the device. This was the applied signal during cool down, once at base temperature to reduce heating through excitation by the voltage the 100 kΩ resistor was replaced with a 1 MΩ resistor, resulting in 10 μV excitation signal. The output signal was connected to a current-voltage amplifier using an amplification of 1 x 10^7 V/A and monitored through a lock-in connected to the computer using a GPIB connection. The CyroMeas software package was used to recover the signal, this

is designed to be used via LabView by Dr Christopher Ford, see figure 5.2.

Figure 5.3 shows the differential conductance as a function of split gate voltage for device A as it is cooled down from 4.2 K to 38 mK. The conductance data taken during cool-down of both devices shows a 0.7 G_0 structure which is known to be spin related [67]. The 0.7 structure is more pronounced at 4.2 K and there is a hint of it at base temperature. The origin of the 0.7 anomaly is still subject to debate. Proposed explanations vary widely including ferromagnetic spin coupling [68], Wigner crystallisation [69] and various treatments of inelastic scattering [70, 71]. Among many theories put forward, there is a broad consensus that the 0.7 feature arises from a spontaneous lifting of spin degeneracy in the QPC [67], as a result of many-body interactions arising from low carrier density, when the conductance is about go to zero, as a result there is a single 0.7 structure on the 1st plateau and there are no harmonics of it on higher plateaus.

In figure 5.3 the first 2 plateaus that correspond to $2e^2/h$ and one at $2(2e^2/h)$ are visible. The plateau at 3 G_0 is screened out, this is probably due to effects such as resonance due to quantum interference caused by impurities, channel wall irregularities or reflections at QPC ends causing quasi-one-dimensional states. The size of the QPC is also a limiting factor, as well as the flatness of a quantisation plateau, which depends on the geometrical aspect ratio (W/L) of the QPC channel.

We have illuminated the devices using a red LED in order to get a conductance of around 800 μS, corresponding to 4.3 x10^5 $Vcm^{-2}s^{-1}$. By illuminating we increase the carrier density as well as electron mobility of the device, which increases the electron mean free path to 2.3 μm thus reducing the UCF's seen in earlier devices.

Device B showed defect-free ballistic conductance, this device has a length of 200 nm and a width of 400 nm. As this device is wider, we are able to see plateaus up to 6 G_0. Figure 5.4 shows the differential conductance as a function of split gate voltage during cool down of the wider gate device (device B), once again the 0.7 structure is visible and more pronounced at higher temperatures.

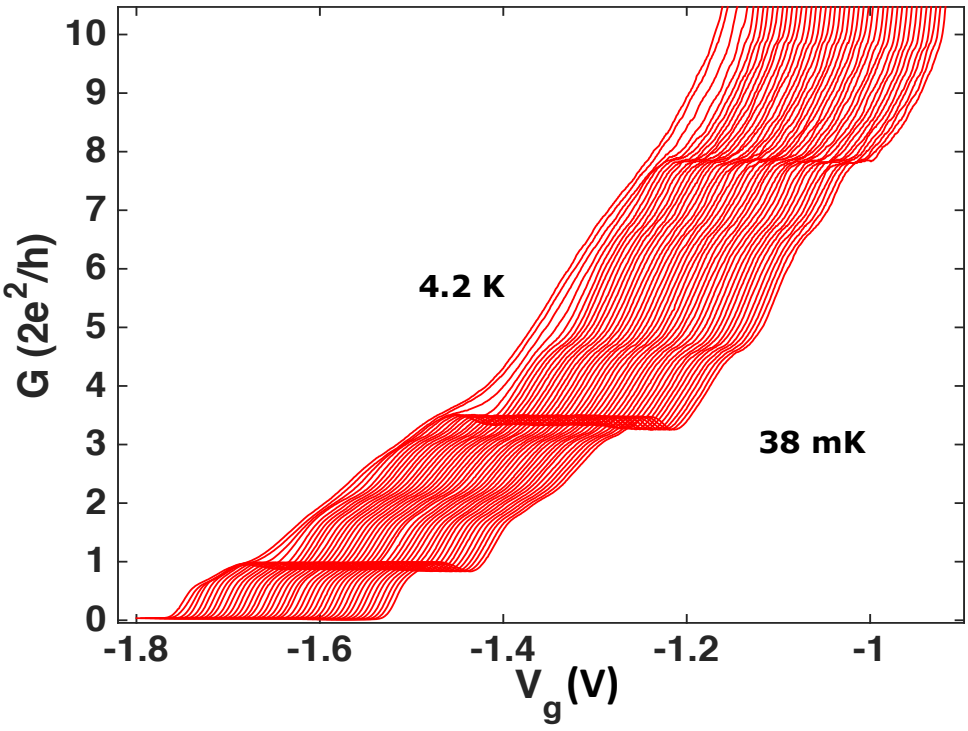

Figure 5.3: Differential conductance as a function of split gate voltage during cool down for Device A (L= 40 nm W= 100 nm). Data has been offset horizontally for clarity.

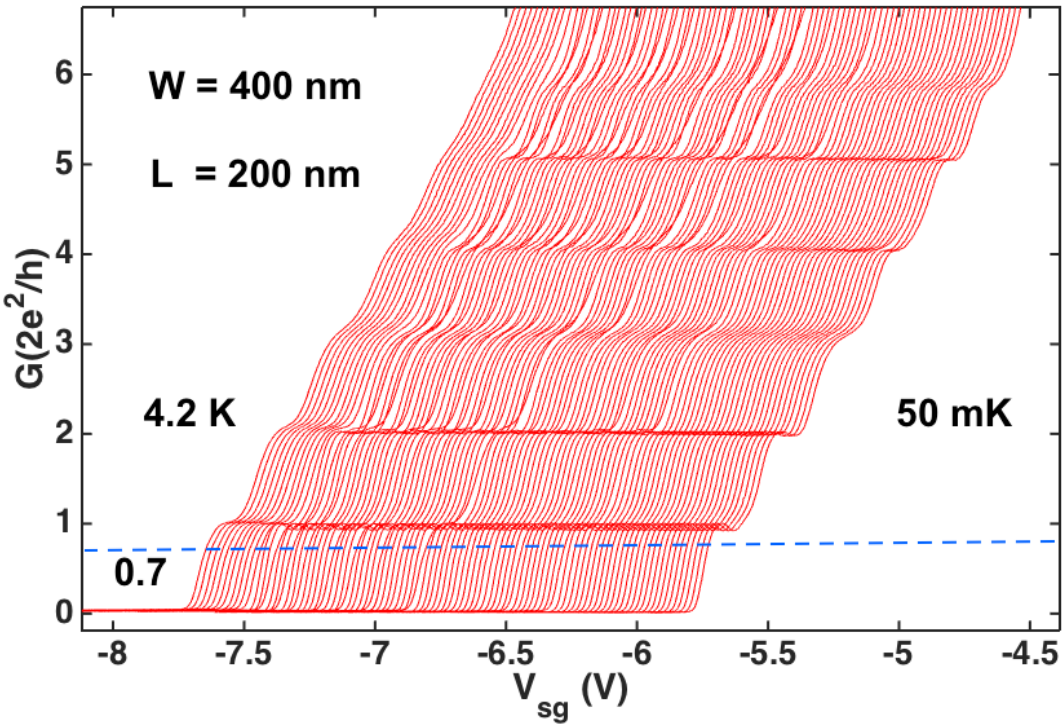

Figure 5.4: Figure showing how the differential conductance progresses during cool down from 4.2 K to 50 mK for device B (L=200 nm W= 400 nm). Data has been corrected for series resistance and offset horizontally by 0.025 V for clarity.

5.3.1 Determining the *g*-factor

To determine the Landé g factor we have used the method developed by Patel *et al.* [63], which combines the measurement of the splitting due to the source-drain bias $\delta V_g/\delta V_{sd}$ with measurements where splitting is due to the field $\delta V_g/\delta B_{\|}$. However the sign of the g factor cannot be determined using this method. Earlier studies have shown that the g value is enhanced in 1D compared to the bulk value[63, 72], and that g changes significantly between 1st subband and consecutive subbands [63, 72]. The subband energy is obtained by observing the splitting in gate voltage due to an applied d.c. source drain bias V_{sd}, which gives us the subband spacing as a function of gate voltage $\delta V_g/\delta V_{sd}$. The energy difference between spin split energy levels is defined by the Zeeman energy E_z. The splitting in field is visible where $E_z = -g\mu_B B > k_B T$ (see fig. 5.6b). These combined give an estimation of the effective g-factor.

$$|g^*| = \frac{1}{\mu_B}\frac{d(\Delta E_z)}{dB_{\|}} = \frac{1}{\mu_B}\frac{d(\Delta E_z)}{dV_g}\frac{dV_g}{dB_{\|}} = \frac{e}{\mu_B}\frac{\delta V_{sd}}{\delta V_g}\frac{\delta V_g}{\delta B_{\|}} \tag{5.1}$$

Where μ_B is the Bohr magneton, E_z is the Zeeman energy and g^* is the effective g-factor. From figure 5.6 the subband spacing is shown to be between 3.6 meV and 2.5 meV. Larger values were reported in $In_{0.75}Ga_{0.25}As/InP$ [72]. However, these devices were etched wires, which usually require a perpendicular magnetic field in order to reduce the disorder in the system and achieve quantised conductance[63]. The term $\delta V_g/\delta B_{\|}$ can be estimated from figure 5.6b. We obtain an enhanced g-factor of 6.5 for n = 1, which is higher than previous studies [72], and the data is obtained in the absence of Landau quantisation using in-plane magnetic field.

In a 2DEG considering a free-electron model, and applying a spin-orbit interaction to surface states that are localised in the near surface plane, the free-electron parabolic dispersion will be split in two parabola, shifted in k direction with energies

$$E_{1,2} = \frac{\hbar^2 k^2}{2m} \pm \alpha\hbar k \tag{5.2}$$

where α is the Rashba parameter, for the 2DEG system we have used 0.67 x 10^{-11} eVm, and a Rashba spin-orbit coupling energy E_{Rashba} of 2.2 meV [19]. If the Rashba spin-orbit coupling is included in the calculation of the effective $|g*|$ factor, this reduces it to 6. The reduction is due to the competition of Rashba and Zeeman fields.

5.3.1.1 Source drain bias

A d.c. voltage was applied to the source drain bias using device B at 50 mK. The d.c. source drain bias caused additional plateaus to appear at half integer values. The differential conductance in the non-linear regime was first calculated by Glazman and Khaetskii [73] and later by Martin-Moreno *et al.* [74]. This has also been observed in previous studies investigating the link between the spin degenerate 0.5 structure with the 0.7 structure [75]. D.c. bias spectroscopy was performed on the device by stepping the d.c bias from 8 mV to -8 mV in 0.025 mV increments. This is shown in figure 5.5. In GaAs devices under similar conditions a 0.25 plateau usually forms rather than 0.5 and has been previously explained as a Coulomb Blockade feature [7, 76]. The 0.25 G_0 feature has been recently explained as source drain bias lifting the momentum degeneracy resulting in a unidirectional ferromagnetic order [60]. There are also some anomalous plateaus in the current data that show up at 0.85 and 1.7 G_0 in the conductance plot.

An interesting feature of this d.c bias spectroscopy is the fact that it is asymmetric between positive and negative bias. While positive d.c bias has a 0.5 structure that stays strong with increasing d.c. bias, there is a 0.25 structure that develops at negative d.c. bias (see fig. 5.5). This asymmetry could be from self-consistent electrostatic effects close to pinch-off, or it could be caused by lateral spin-orbit coupling due to a small asymmetry in the confining potential [77]. This asymmetric appearance of the 0.25 G_0 could also mean that a total spin polarisation is energetically unfavourable, and that rather a spin density wave, skyrmion forms, this results in an in-plane ferromagnetic ground state, i.e., in which the pseudo-spin magnetisation is constrained in the xy plane. Instead of forming a pair of spin-split Landau levels, electrons coexist in one level, hence adopt lower-energy, in a spin-wave configuration such that no electron is neighboured by another with identical spin. This has been known to happen in silicon in a magnetic field where an interaction induced spin polarisation can be observed [78], it has also been observed in $Al_{0.13}Ga_{0.73}As$ systems [79]. When the wave forms, neighbouring electrons have spins which are just canted very slightly hence the charge repulsion is low. This can also explain the lower values of g measured.

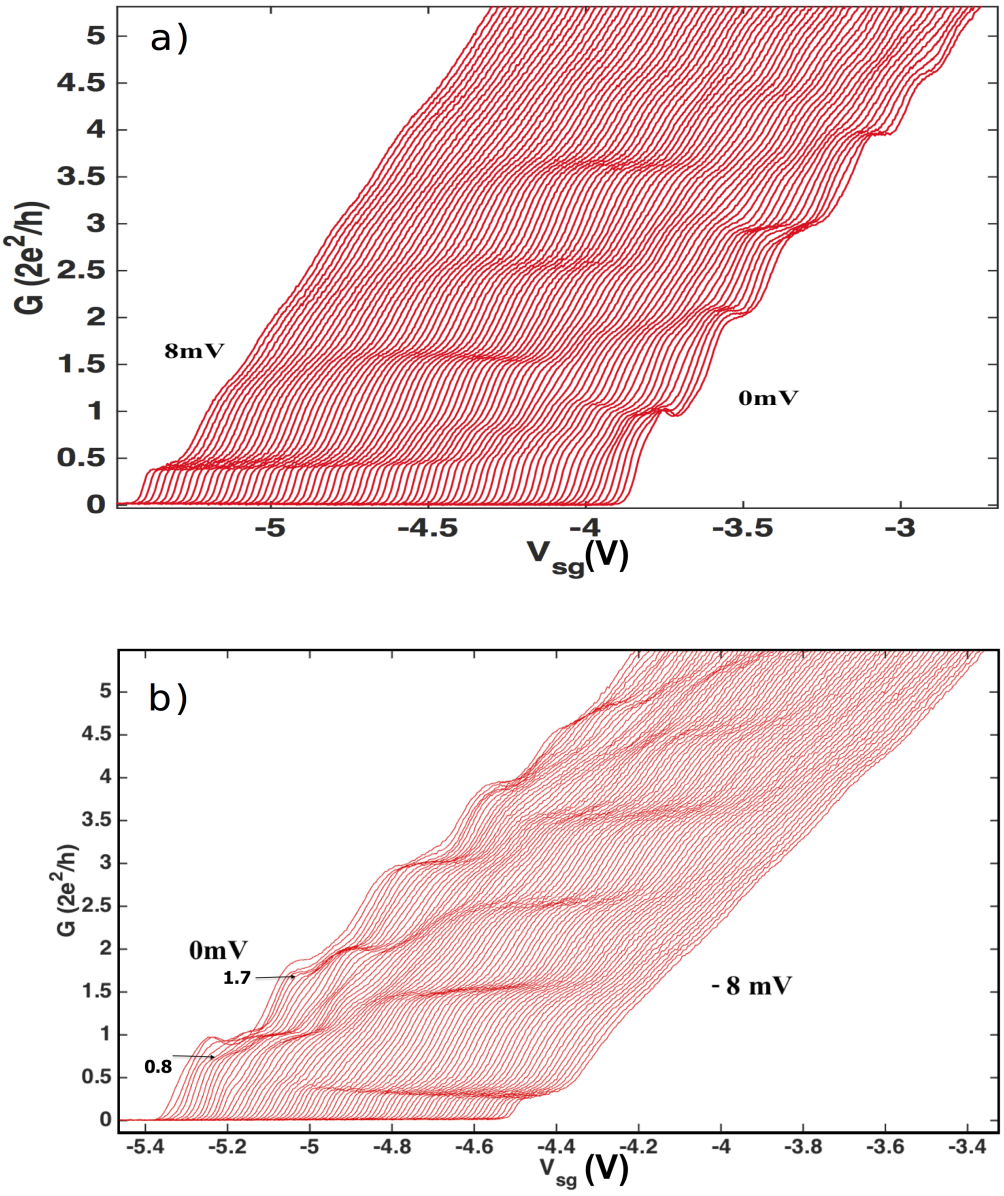

Figure 5.5: **a)** d.c, bias spectroscopy of device B from 0 mV to 8 mV, the 0.5 ($2e^2/h$) is observed and remains from around 3 mV. At 3 mV plateaus are present at 0.5, 1.5, 2.5 and 3.5($2e^2/h$). **b)** d.c, bias spectroscopy of QPC device from 0 mV to -8 mV, the 0.5 ($2e^2/h$) is observed around 3 mV, but tends to go below 0.5 ($2e^2/h$) to 0.25($2e^2/h$) as the d.c bias is increased to -8 mV.

5.3.2 Transport measurements in magnetic field

1D transport measurements in a parallel magnetic field show that in contrast to GaAs [80], only small magnetic fields i.e 1.5 T are required to lift spin degeneracy in InGaAs devices, this is due to the large Rashba spin orbit coupling and high g factor in these systems. The orientation (applied field perpendicular to the Rashba field), was chosen to maximise the effects of the Rashba field.

Figure 5.6 a) shows a greycale plot of d.c. bias measurements at zero field and figure 5.6 b) shows the Zeeman splitting for the subbands of the QPC from zero field to an 8 T parallel field respectively. Our devices required only 1.5 T of in-plane field to lift the spin degeneracy compared with 6 T (from Ref. 28). This is much lower than previous studies of $In_{0.75}Ga_{0.25}As$ QPCs [72]. From the figure we can see that the Zeeman splitting is very clear and $\delta V_g/\delta B_{\|}$ can be easily estimated from it.

Using the results from the measurements from source drain bias and Zeeman splitting from in-plane magnetic field measurements, g-factors were calculated for the first three subbands. Table 5.1 shows the calculated g factors for our device. In the first subband the g-factor is 6.5 which is order of magnitudes higher than GaAs which has a g-factor of 0.44.

The g-factor measured in a QPC by source-drain bias spectroscopy is usually significantly larger than its value in a 2DEG. There has been some theoretical work to explain this. Reference [81] attributes the g-factor enhancement to Landau Fermi liquid exchange interaction mechanism in an infinitely long quantum wire. Although the length of the quasi-1D channel connecting the leads is usually much shorter than the spin relaxation length. Reference [82] links the enhancement to magnetic splitting enhancement. However ref. [83] shows that this effect cancels outs in a source-drain bias spectroscopy, and explain the enhancement mechanism in a theory accounting for the Hartree and Fock electron-electron interaction, and show that the effect lies on the non-equilibrium nature of the spectroscopy at finite bias.

Parameter	n=1	n=2	n=3
$\delta E_{n,n+1}$ (meV)	3.8 $\pm$0.6	2.9 $\pm$0.6	2.5$\pm$0.6
$\delta V_g/\delta B_{\|}$ (V/B)	0.016 $\pm$0.005	0.021 $\pm$0.004	0.022 $\pm$0.006
$e\delta V_{sd}/\delta V_g$ (meV/V)	23	17.13 $\pm$0.9	12.85 $\pm$0.8
$\|g^*\|$	6.5	6.2	4.9

Table 5.1: Table showing the calculated values of $|g|$ factor.

In this measurement when an in-plane magnetic field is applied along the quantum

wire a reduction in g-factor is observed from the measured 2D value of ~ 9 to 6.5 in the lowest subband when the Rashba field and the applied magnetic field are perpendicular. This reduction is one of the manifestations of the Rashba spin-orbit coupling effect that creates an effective magnetic field perpendicular to the applied field, pinning the spin angular momentum in this direction for applied fields up to $\sim$ 4T [19].

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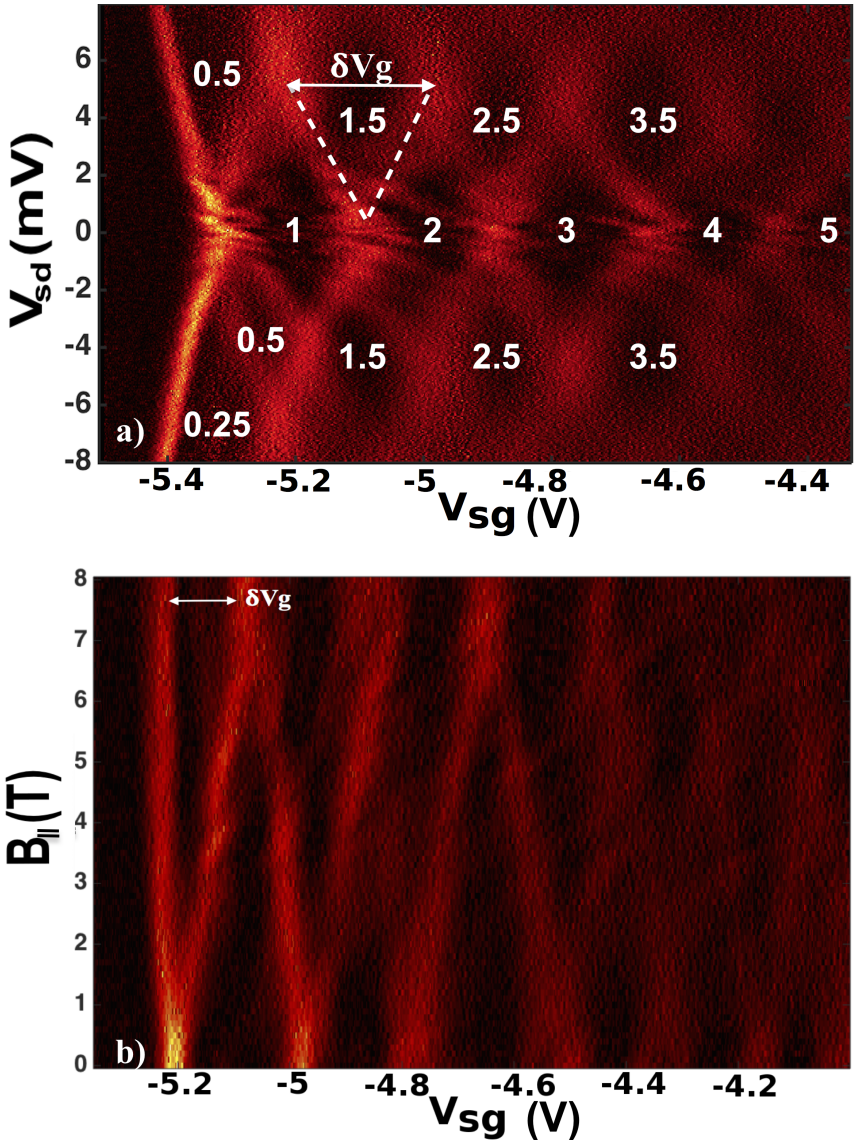

Figure 5.6: **a)**Transconductance dG/dV$_g$ plotted against source-drain bias V$_{sd}$ at B=0. Regions of bright orange and red correspond to a large amplitude of dG/dV_g, indicating the locations of subband transitions. **b)** Transconductance dG/dV_g as a functions of split gate voltage V_{sg} and magnetic field $B_{||}$. Regions of orange and red indicate a large amplitude of dG/dV_g corresponding to locations of subband transitions.

5.3.3 Lateral Bias

Asymmetric split-gate biasing was applied by stepping one gate voltage and sweeping the second, see figure 5.7. In this measurement one of the split gates was swept from depletion with the other split gate held constant. The latter gate was then stepped by 20 mV towards depletion and the former gate was swept again. This was repeated with the latter gate becoming increasingly depleted. The results can be seen in figure 5.7. We observe a weak 0.5 G_0 plateau appearing but this increases to 0.75 G_0 as the channel is made more asymmetric. In addition there are plateaus which appear at 1.5 and 3.5 G_0 as the channel is made more asymmetric. The 0.5 plateau shifts towards 0.75 G_0 with the spatial variation of the channel between the split-gates. The 0.5 G_0 plateau was observed in InAs quantum well sandwiched between $In_{0.53}Ga_{0.47}As$ barriers, when the confining potential was made sufficiently asymmetric [39]. However the measurements in ref. [39] were made using etched channels with side gates. The etched wires where the edges are exposed introduces roughness and more disorder, but the spin-orbit length is smaller due to stronger confinement[84]. Spin polarisation can be triggered by lateral spin-orbit coupling and lead to fully spin polarised state in the presence of strong electron-electron interaction [39].

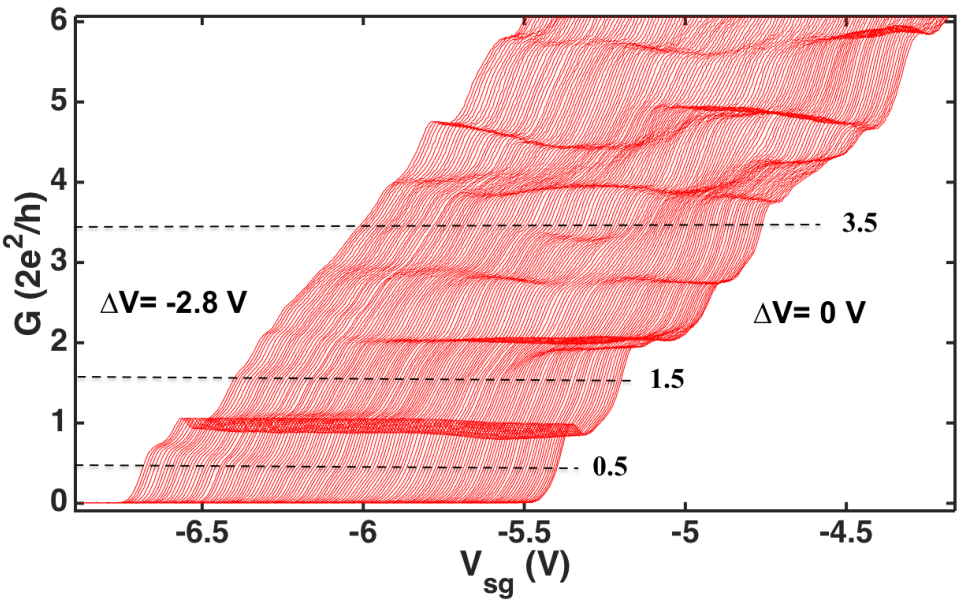

Figure 5.7: Asymmetric bias to the split-gate with one gate held constant and the other gate shifted incrementally up to ΔV = - 2.8 V at 50 mK in steps of ΔV = 20 mV.

5.3.4 Summary

In this Chapter we have summarised the low temperature measurements of high quality split gates fabricated from W436 wafer. Clear conductance plateaus were observed using narrow split gates, and comparable data to high quality GaAs devices have been obtained using $In_{0.75}Ga_{0.25}As$ wafers grown in the Cavendish Laboratory. We have also shown that the high g factor value in these devices make it easier to observe spin orbit interactions. The experiments have helped us to choose an ideal length scale to stabilise quantised conductance with minimal effects from disorder, due to impurities. We have shown that the g is enhanced in the lowest subband. These experiments have shown that narrow split gate devices are essential for observing ballistic effects in $In_{0.75}Ga_{0.25}As$ devices, and demonstrated that $In_{0.75}Ga_{0.25}As$ QPCs are suitable for future spintronic devices that require only minimal magnetic fields. In this low disorder system no perpendicular magnetic field is needed to observe conductance plateaus at $2e^2/h$. It is shown that there is a reduction in backscattering due to spin-orbit coupling, leading to enhanced ballistic quantisation up to 6 G_0. In the measurements we see that when an in-plane magnetic field is applied along the quantum wire a reduction in g-factor is observed from the measured 2D value of $\sim$ 9 to 6.5 in the lowest subband when the Rashba field and the applied magnetic field are perpendicular.

In the next chapter we introduce p-Ge two dimensional hole gas systems, and demonstrate quantised 1D transport in these systems, and investigate many body effects at low carrier densities.

Chapter 6

Ballistic transport in p-type Ge

6.1 Introduction

In chapter 5 we have seen the effects of Rashba SOI in $In_{0.75}Ga_{0.25}As$ in 1D transport measurements. In this chapter we introduce a completely different system to group III-V semiconductors. This chapter introduces Ge 2DHG system. In the 1D regime we have no Rashba field and SOI is very small in these systems as Dresselhaus spin-orbit interaction due to bulk inversion asymmetry is absent [32]. The effective mass of the heavy holes (0.06 m_e) makes it comparable to electrons to GaAs. We have used high mobility Ge Hole gas systems grown in University of Warwick. The motivation behind this work was simple, 1D transport in Ge QW's in literature is very limited, the main reason behind this was the wafer quality. Now that high mobility wafers are available we have decided that it would be a good comparison to $In_{0.75}Ga_{0.25}As$ wafers used in this project, and it gives another exciting pathway for spintronic research to use group IV systems as the industry is more suitable. We have carried out 1D transport measurements on split gates fabricated using p-Ge wafers and split gates with top gates at 20 mK. This chapter summarises the transport measurements carried out in this system.

6.2 Properties of the two-dimensional hole gas

CMOS compatible nanostructures in p-type Ge have developed rapidly but without the observation of ballistic effects that are characterised by quantisation of the electrical conductance [85]. This has been partly due to material quality, however recent improvements in SiGe growth technology with reduced background impurity levels and

Figure 6.1: Schematic of un-doped Ge wafer. Layers not up to scale.

the introduction of thin Ge quantum well layers into $Si_{0.3}Ge_{0.7}$ barriers have achieved hole mobilities (μ) $\sim$ 4500 cm^2/V.s at ambient temperature and at low temperature $> 10^6$ cm^2/V.s, exceeding most state-of-the-art III-V devices [86]. The undoped Ge structure used in this project was grown on a standard Si (001) substrate with 2.3μm of $Si_{0.3}Ge_{0.7}$ buffer layer, followed by 11 nm of Ge QW, and 70 nm of $Si_{0.3}Ge_{0.7}$ and capped by 3 nm of Ge (see fig. 6.1). The wafers were grown using reduced pressure chemical vapour deposition (RP-CVD) system. The quantum well is compressively strained with respect to the $Si_{0.3}Ge_{0.7}$ barriers and the estimated strain in the Ge quantum well layer is 1.2% with respect to the $Si_{0.3}Ge_{0.7}$ barrier. In practice the strain can be less than this due to the SiGe layer not being fully relaxed (but under a partial tensile strain) and also Ge segregation can occur during growth. The measured strain is $\sim$ 0.65% for a different barrier composition of $Si_{0.3}Ge_{0.7}$ in structures but with a similar buffer layers and substrates [87].

The band structure of the undoped Ge quantum well was modelled using the 8 band k.p self-consistent device simulator nextnano^3. Figure 6.2 shows the nextnano^3 [88] solution of the valence band at -1 V forward bias with an SiO_2 gate dielectric.

The band off-set between the Ge quantum well and the $Si_{0.3}Ge_{0.7}$ barriers for the

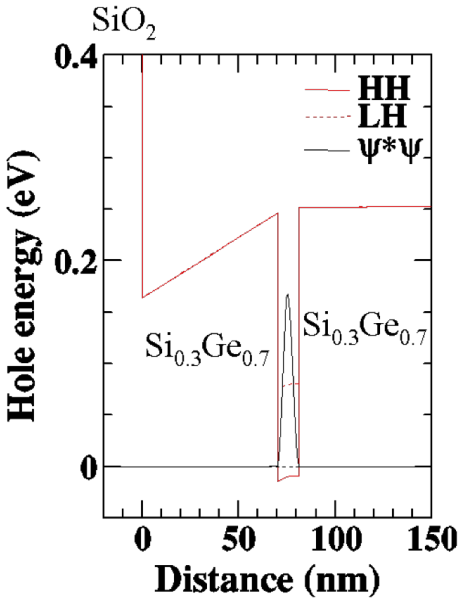

Figure 6.2: The potential profile of the Ge quantum well with -1 V on the SiO_2 insulated surface gate (HH is the heavy hole and LH the light hole states).

heavy hole ground state is ~ 0.26 eV. The solid black line in fig. 6.2 is the self-consistent charge distribution with confinement to the 11 nm thick Ge quantum well. The heavy hole forms the ground state with the unoccupied light hole state 94 meV higher in energy with 1.2% strain for the Ge well, $Si_{0.3}Ge_{0.7}$ barrier combination. In a standard Hall bar the hole density after illumination is 1.28 x 10^{11} cm^{-2} with a mobility of 450 000 cm^2/V.s at 350 mK. There is no indication of parallel conduction in the wafer. The heavy hole effective mass has been determined in similar wafers [89] to be 0.065 m_e at a carrier density of 2 x $10^{11} cm^{-2}$, where m_e is the free electron mass, this is very similar to effective mass of electrons in GaAs wafers (0.067 m_e)[22]).

6.2.1 Spin in Hole Gases

The electrons in the conduction band of III-V semiconductors such as GaAs are characterised by a spin-1/2. However holes in the valence band have an effective spin of -3/2 [90]. This gives rise to many interesting features that are not present in the simpler case of electron systems with spin-1/2. The electrons in the conduction band of semiconductors such as GaAs are described by s-like atomic orbitals [91], the electrons have a total angular momentum j=1/2 that behaves analogously to a spin s =1/2. However

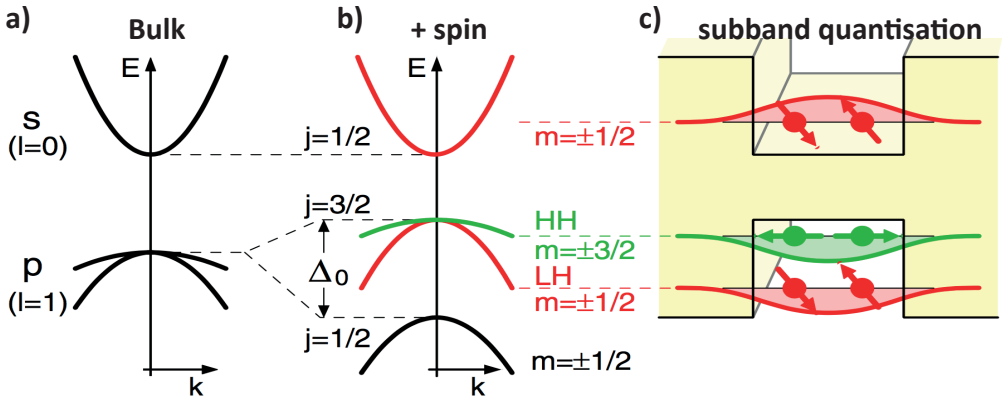

Figure 6.3: Illustration of band structure of GaAs close to the fundamental gap **a)** The electrons in the conduction band described by s-like atomic orbitals taking spin into account the conduction band states are characterised by a total angular moment J=1/2 **b)** Holes in the top of the valence band are described by p-like atomic orbitals, the valence band states are characterised by j =3/2 and j=1/2 states are separated by a spin-orbit gap Δ_0. **c)** In 2D systems the j=3/2 states are split into HH and LH states, the HH states are predominantly made of m= $\pm 3/2$ states with a spin quantisation axis perpendicular to the 2D plane. Figure adapted from Reference [92].

holes are described by p-like atomic orbitals, and have a total angular momentum J = 3/2 and J = 1/2, which are separated by atomic spin orbit gap Δ_0. This results in an effective spin j=3/2 with the states in the top of the valence band. At nonzero wave vectors k the fourfold degenerate states j= 3/2 splits further into HH and LH states (see fig. 6.3).

The ground state wavefunction of the 2DHG is from the heavy hole band, with total angular momentum (J) 3/2 aligned along the out-of-plane strain axis with component (J_z) $\pm 3/2$. The LH states (J=3/2, J_z =$\pm 1/2$) in the valence band are higher in energy by $\sim$ 94 meV from the heavy hole state, so any applied current is only carried by heavy hole states, irrespective of the measurement temperature or applied gate voltages. The compressive strain is fundamentally important in the p-Ge system as it provides the quantisation axis for J along the growth direction perpendicular to the conducting plane. There is no Rashba spin-splitting in the two dimensional contact regions as $J.k_{\parallel} = 0$ and $\Delta\ E_{Rashba} \sim (J \times k_{\parallel}).E_z = 0$, where E_z is the electric field in the growth direction, $k_{\parallel}$ is the linear momentum vector in the plane of the two dimensional hole gas (2DHG) contact regions (with components k_x and k_y). In the 2DHG only a Zeeman spin splitting is observed[93] for large Δ. A cubic ($k_{\parallel}^3$) dependent Rashba has been

Property	Device Set		
	A	**B**	**C**
SiO_2 thickness nm	70	40	40
Gate dimensions :			
Length (nm)	200	100-400	200
Width (nm)	375 - 475	500 - 1000	400
Top gate dielectric	no top gate	pmma (*)	pmma(*)

Table 6.1: A summary of the structural properties of the devices measured in this project. (*) polymethylmethacrylate, an electron beam polymer resist.

previously identified [94, 95, 96] in p-Ge but this effect is too small to be observed in the wafers measured here due to the low carrier density and large compressive strain.

6.3 Device parameters

We have fabricated a series of surface gated devices on the un-doped Ge HEMT structure, following the procedure outlined in chapter 3. Initially we have fabricated simple split gate structures, with a length of 200 nm and a width varying from 375 to 475 nm, on a 70 nm of SiO_2 deposited on the surface due to absence of Schottky barrier. These were measured at 4.2 K down to 380 mK. Due to the thick oxide layer and narrow gates the gates have depleted before the 1st quantised plateau could be observed. The next set of devices had a 40 nm SiO_2 layer, and a wider split gate devices along with top gates.Table 6.1 summarises the devices fabricated and measured in this project.

Initial assessments of the devices fabricated were carried out at 4.2 K at the dip station. Further characterisations were carried out using cryostats at CRL at 1.6 K and 350 mK. Measurements at 20 mK were carried out using Triton 200 at LCN. The conductance signal (G) was measured using a small a.c voltage excitation (V_{sd}) typically 10 to 20 μV at 33 Hz. A current pre-amplifier was then used with a gain of 1μA/V. The differential conductance dI/dV_{sd} was taken from the signal at the lockin amplifier. The d.c source drain voltage measurements were made by adding a d.c voltage through a potential divider to the a.c signal, varied between 0 to $\pm$5 mV. The d.c current was not recorded in these measurements. The devices were illuminated in-situ either by a red or an infra-red LED. This was required to create a persistent photoconductivity effect.

6.4 1D transport in Ge Split gates at low carrier density

In general, quantised conductance in a ballistic split-gate device is observed in the differential conductance (G) at values $g_v g_s Ne^2/h$, where g_s is the spin degeneracy, g_v is the valley degeneracy, N is the (integer) number of one-dimensional channels defined between the split-gates; e and h are the unit of charge and Planck's constant respectively [4, 97]. In n-type strained Si/SiGe etched narrow channels and quantum point contacts, a valley degeneracy (g_v) of 2 was observed [98, 99] with quantised conductance plateaux separated by 2 G_0. This valley degeneracy could be removed by strong in-plane confinement [100] with plateaux then separated by G_0. The valley splitting can be larger than the spin splitting [101]. In contrast to the conduction band, the heavy hole valence band in Ge has only a single valley at the Γ point with g_v =1. In self-assembled p-Ge core, Si -cladding nanowires a weak ballistic feature was identified among classical Coulomb Blockade features and with suppressed back scattering in this particular device, ballistic effects could in principle be observed to high temperatures [102]. Although there has been no experimental report of quantised conductance in p-Ge/SiGe wafers, the conductance of the one-dimensional hole gas has been predicted to be partially quantised depending on the energy Δ, the light and heavy hole splitting [103]. This model predicts a modified ballistic conductance staircase dependent on the exchange interaction being either ferromagnetic or anti-ferromagnetic with just a single plateau at 0.5 G_0 for large Δ (> 10 meV), irrespective of the sign of the exchange interaction. This is the experimental situation investigated here where Δ is calculated to be ∼ 94 meV. This was the observed case in our initial measurements with thick oxide layer and narrow gates.

Figure 6.4a shows the differential conductance data at 1.7 K and 350 mK as a function of split-gate voltage. In the figure a strong 0.5 G_0 is visible, confirming the prediction by ref. [103], along with a structure at 0.7 G_0. The channel definition voltage is at 0.8 V in this device, with a 1D conductance definition (G_d) < G_0, this is due to narrow gate along with thick (70 nm) SiO_2 dielectric layer. The ballistic nature of these channels were confirmed by applying a d.c voltage to the source drain. Figure 6.4b shows the d.c bias spectroscopy from 0 mV to 4 mV. The 0.7 G_0 structure disappears with applied V_{sd} (∼ 0.4 mV) and the 0.5 G_0 is replaced by a 0.25 G_0 plateau at ∼ 0.6 mV. The appearance of 0.25 G_0 structure is consistent with the studies of 1D channels in GaAs devices [60]. Figure 6.4c shows asymmetric biasing. For this measurement split-gate 1 was swept from depletion with split-gate 2 stepped in 10 mV increments towards depletion. The 0.5 plateau does not shift dramatically with the

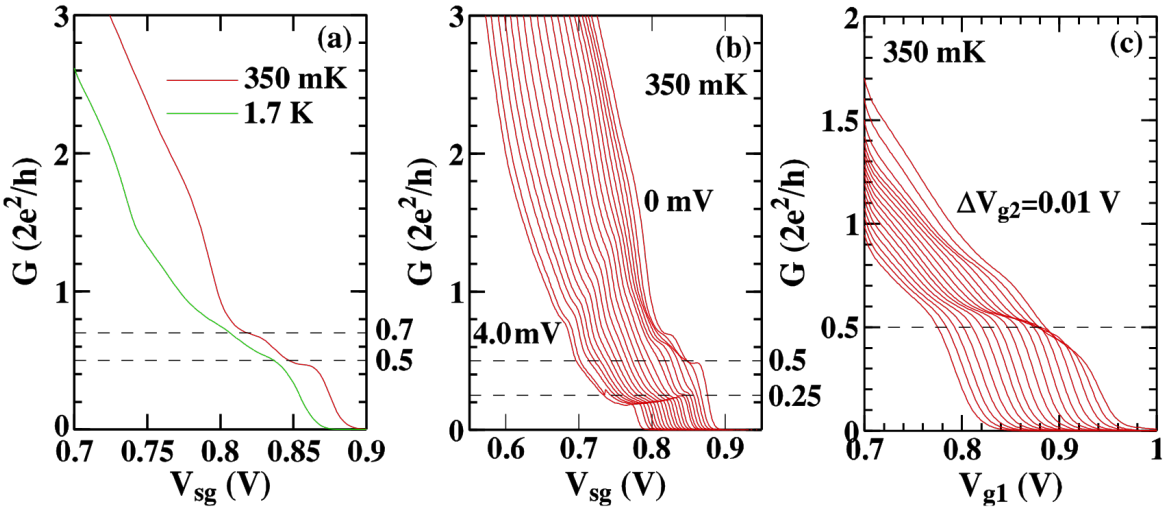

Figure 6.4: Transport measurements for device A **a**) The differential conductance as a function of split-gate voltage at 1.7 K and 350 mK with Vg1 = Vg2 for device A. **b**) The differential conductance as a function of split-gate voltage adding a d.c bias from 0 to 4 mV in steps of 0.2 mV. **c**) Applying an asymmetric split-gate voltage (with $V_{g1} \neq V_{g2}$) shifting the pinch-off voltage by a total of -0.15 V in 10 mV increments.

spatial variation of the channel between the split-gates. However, for a LSOC induced spin splitting the 0.5 plateau should be dependent on the asymmetric bias or E_y field. In fact in high mobility $In_{0.75}Ga_{0.25}As$ 1-dimensional channels it was observed [101] that asymmetric biasing did remove structure (due to an impurity or a resonance) close to the spin-split 0.5 G_0, however this effect is not observed in this set of devices. There are 2 definition voltages (V_{d1} and V_{d2}) in defining the 1-D channel in this system. This is due to the different carrier densities under the optical metal gates compared to that under the e-beam defined metal gated regions of the device after illumination. In device A, V_{d1} is 0.7 V and V_{d2} is 0.8 V and ΔV_d (= V_{d2}- V_{d1}) agrees with the difference in carrier densities measured in the 2DHG where p1 = 1.28×10^{11} cm^{-2} (under the e-beam defined gate or the ungated 2DHG) and p2 = 1.0×10^{11} cm−2 (under the thicker optically defined gate) and the geometry of the device for 70 nm thick SiO_2. This difference in carrier density predicts a ΔV_d of 0.12 V compared to 0.1 V observed in device A confirming the carrier densities in the patterned gate device.

The next set of devices had a 40 nm SiO_2 dielectric layer and had a global top gate to allow the carrier density to be changed in the 1-D channel. Figure 6.5 shows an illustration of the device along with an SEM image. Measurements at 4.2 K and 2.4

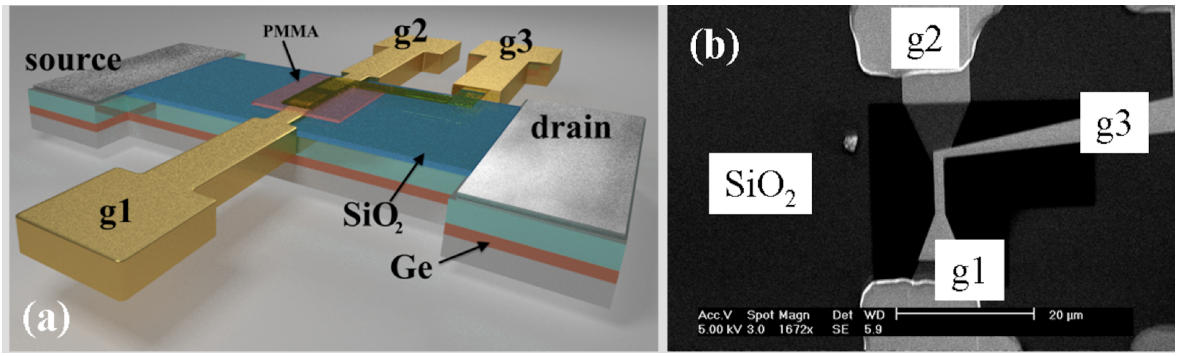

Figure 6.5: **a**) The overall device scheme. The patterned gates g_1 and g_2 define (V_{sg}) the 1-dimensional channel and the global top gate g_3 controls the carrier density in the channel **b**) An SEM image of a patterned gate region showing the pmma top gate dielectric underneath the g_3 Ti-Au metallisation.

K have confirmed that the definition voltage was at G > G_0. Figure 6.6a shows the conductance data for device B at 4.2 K and 2.4 K. The definition voltage is at ∼ 0.5 V, and the channel is defined at G_0 > 5 G_0. At 4.2 K there are no plateaux visible around 0.5 G_0, and at 2.4 K, there is a strong plateau at 0.5 and a hint at 1.5 G_0. Figure 6.6b shows the dc bias spectroscopy from ± 3 mV, this shows clear plateaux at 0.25 G_0. Further measurements were carried out with this device using Triton 200 at LCN at 20 mK.

Figure 6.7a shows the differential conductance as a function of split-gate bias at 20 mK. The top gate is stepped from 0 V (where p ∼1 x 10^{11} cm^{-2}) to +1 V (depletion with p = 0). In addition to the strong 0.5 G_0 plateau, reproducible plateaux are seen at 1.0 G_0, 1.75 G_0, 2.5 G_0 and 3.0 G_0 due to the wider channel at definition compared to device A. There is no plateau at 1.5 G_0 or 2.0 G_0 but a clear, reproducible plateau at 1.75 G_0. The 0.5 G_0 plateau does not disappear with reducing k_x via the surface gate voltage (V_{tg}). This confirms the applied d.c bias measurement that show the spin-splitting does not switch off at lower carrier density. This is due to the LSOC spin-splitting that is enhanced by hole-hole interactions[104]. A 0.25 G_0 plateau appears (see fig. 6.7a) at ∼ 4x10^{10} cm^{-2} with top gate voltage due to an enhanced exchange interaction removing the momentum degeneracy (between +k_x and - k_x) in the system without a source-drain bias. The 0.7 plateau is suppressed at this measuring temperature. An in-plane magnetic field up to 10 T (introducing a Zeeman energy of 7.4 meV at 10 T for a g-factor of 4 [102]) does not split any plateau, see fig. 6.7b as the valence band states are already spin-split by the LSOC effect in 1-

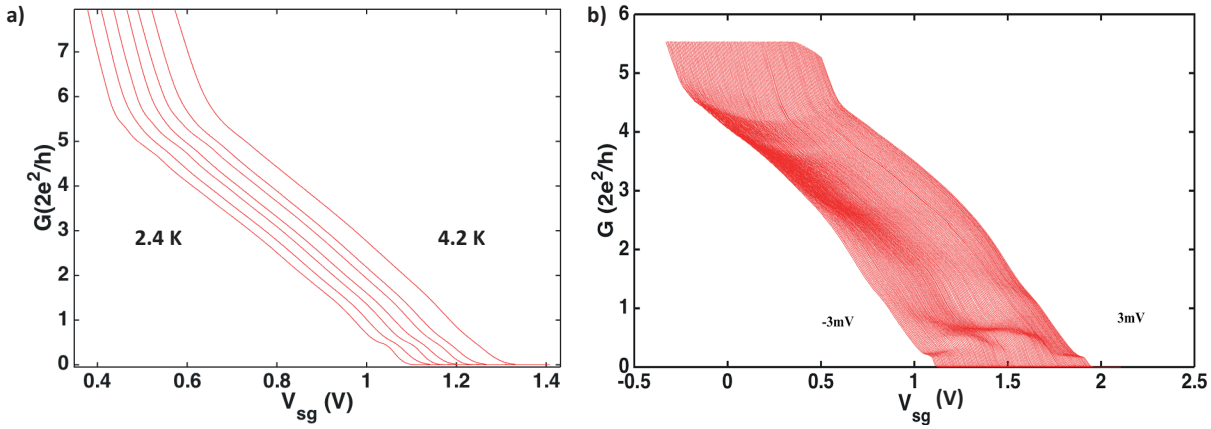

Figure 6.6: **a**) Differential conductance as a function of split-gate voltage at 4.2 K to 2.4 K. **b**) The differential conductance as a function of split-gate voltage adding a d.c. bias from -3 mV to 3 mV.

D. An explanation for the 0.5 G_0 structure seen in the measurements could be that the asymmetric voltage on the split-gates, provides a lateral field E_y that results in a partially spin-polarised system characterised by conductance at 0.5 G_0. In p-Ge an asymmetric confining potential with lateral electric field E_y removes the degeneracy in the angular momentum states J_z , i.e. the spin-splitting is $\sim$ (J x $k_{\|}$).$E_y \neq 0$ and this mechanism accounts for the 0.5 G_0 plateau in the conductance, seen in devices A and B. A lateral spin-orbit coupling (LSOC) effect (as opposed to a Rashba spin-orbit coupling which is due to electric fields in the growth direction) has been observed in n-type InAs quantum point contacts [39, 105] but with spin-polarisation already in the 2-dimensional contact regions due to the Rashba effect.

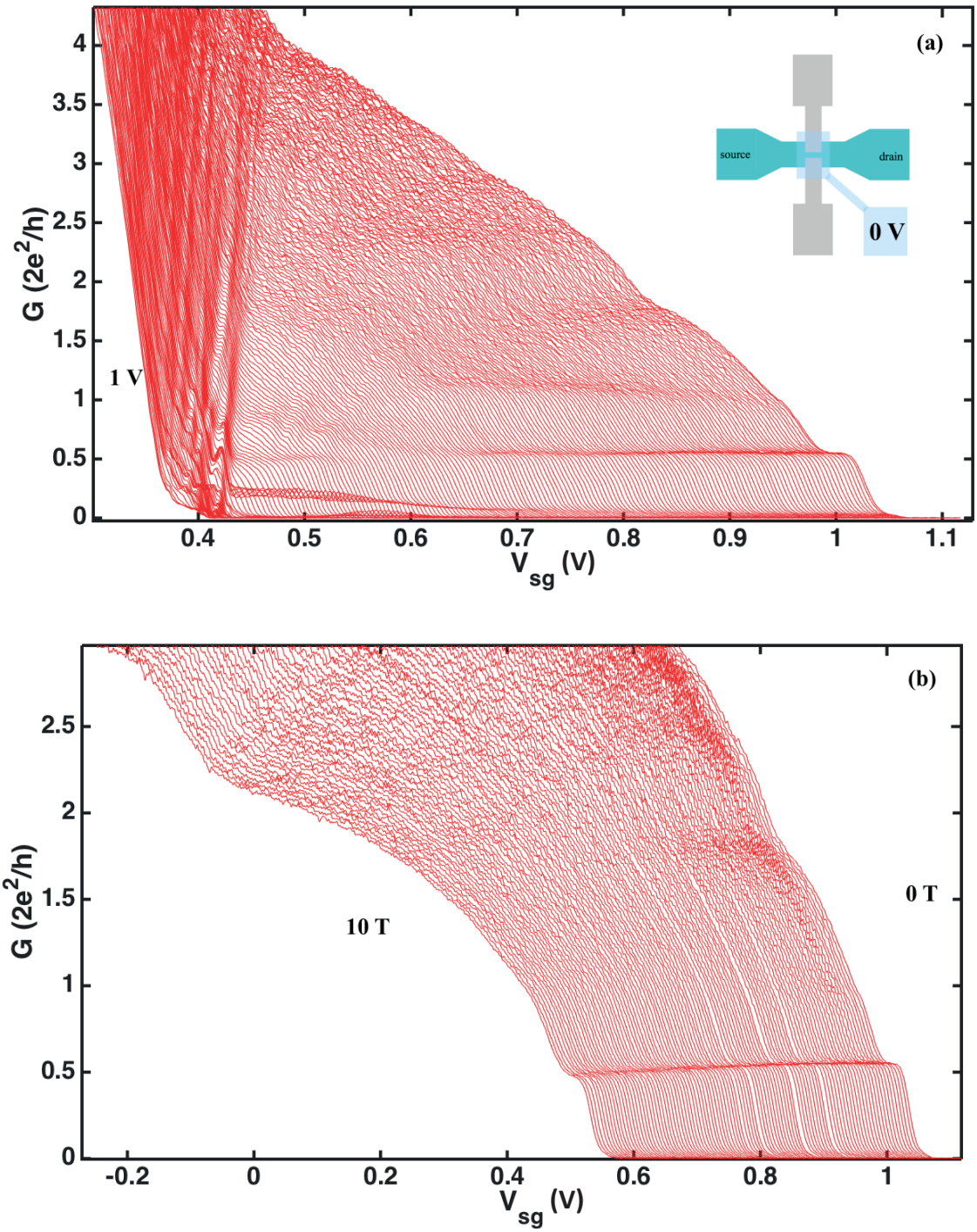

Figure 6.7: **a**) The differential conductance as a function of split-gate voltage at 20 mK for device B. The global top gate voltage is stepped in +5 mV increments from 0 to 1 V (extreme left trace). **b**) The differential conductance as a function of split-gate voltage with B in-plane from 0 to 10 T in steps of 0.1 T at 0 V_{tg}.

6.4.1 Transport measurements on device C

The next set of devices (device C) had a slightly shorter channel width, and all the split gates were identical to allow for a statistical analysis of the devices. These devices have been illuminated for much longer to get a higher carrier density and higher mobility. The mean free path of these devices were 2.1 μm. Figure 6.8 shows the differential conductance as a function of patterned gate voltage at 20 mK in device C. The top gate is stepped from 0V on the right hand side of the figure (where p$\sim 1 \times 10^{11}$ cm^{-2}) to + 1 V (depletion with p$\sim$ 0 in the channel). Reproducible and clearly defined conductance plateaux are seen at up to 7 G_0, in depletion mode with $V_{g3} > 0$. The plateau separation is consistent with spin degenerate, single valley conduction as expected, as opposed to earlier devices, where a strong 0.5 G_0 is seen. The 0.5 G_0 can also be seen here when the top gate voltage is about 0.12 V, suggesting that the low carrier density enhances hole-hole interactions, leading to spin degeneracy to be lifted, and confirming the measurements made with device A and B.

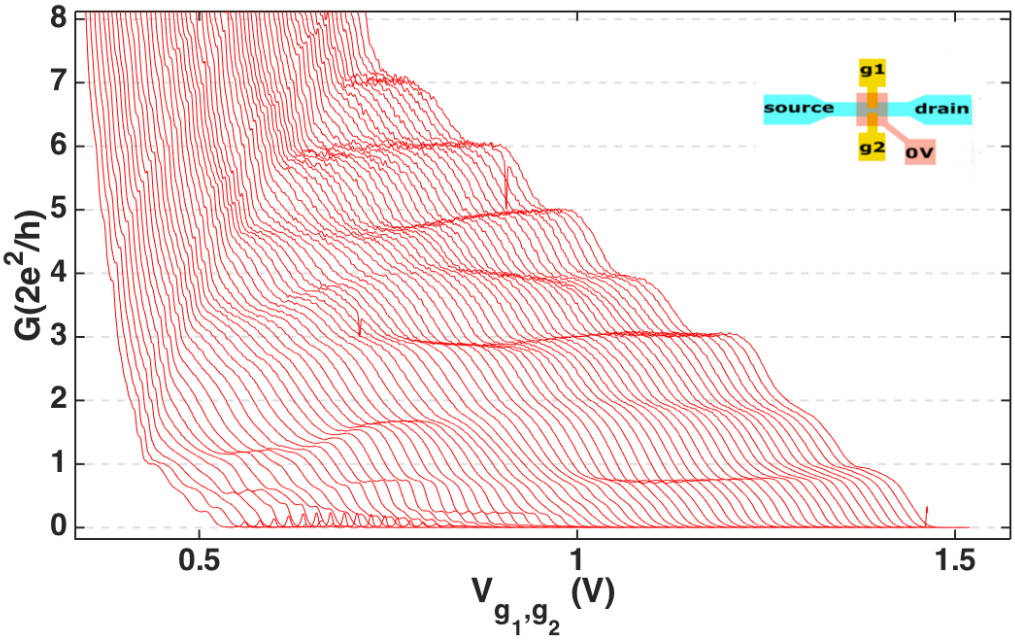

Figure 6.8: The differential conductance as a function of patterned gate voltage at 20 mK. The top gate voltage is stepped in + 5 mV increments from 0 to 1V (on the extreme left).

At conductance < G_0 a shoulder at $\sim 0.7\times(2e^2/h)$ is seen in p-Ge. This feature

is characteristic of clean 1-dimensional channels [67, 106], and eventually weakens here at higher top gate voltages due to disorder caused by an impurity in the channel. The disorder is evident as peaks or shoulders in depletion mode just before the channel pinches-off. Re-illuminating the device can remove this structure. The in-plane g-factor for the p-Ge heavy hole gas is ~ 0 as the angular momentum J is pinned in the growth direction as discussed above (see reference [92]). However, a large in-plane magnetic field (B) removes the degeneracy in the angular momentum $J_z = \pm 3/2$ states, and at $\sim$ 2 T the half-plateaus start to appear from 0.5 to $4.5\times(2e^2/h)$, see fig. 6.9 which shows in-plane fields to 6 T. This is further evidence that the plateau are ballistic with the hole gas showing $g_v = 1$ and $g_s = 1$ in fig. 6.9 under those conditions. The half-plateau although weak appear due to a Zeeman splitting, with a small g-factor, rather than due to a spin-orbit coupling effect that has been seen in InGaAs based materials [39, 76, 104, 107]. A 0.25 G_0 plateau also appears (see fig. 6.8a) at $\sim$ 4x10^{10} cm^{-2} with top gate voltage.

Applying a negative voltage to the top gate increases the carrier density and mobility of the device, in the enhancement mode (see fig. 6.10) the top gate voltage is stepped from 0 V on the left hand side to -0.2 V on the right hand side in increments of -10 mV. In enhancement mode conductance plateaux up to 10 $\times$ $(2e^2/h)$ can be resolved. The changing series resistance with V_{g3} due to the increase in carrier density in the 2DHG contact regions was taken into account.

Applying a d.c. voltage bias between the source and drain contacts of the device removes the momentum degeneracy for the two physical directions for current flow. Figure 6.11a and b shows the conductance of device C as a function of the patterned gate voltage V_{g1} and V_{g2} with a d.c. voltage that is incremented from 0 to $\pm$ 5 mV. The two figures are symmetric with d.c. voltage as expected from the starting point (on the left hand side of the figures) showing integer plateaus up 7 G_0. The integer plateaus have gone by $\sim \pm$ 1 mV and for $G < G_0$ stable plateaus has developed at 0.5 G_0 and 0.25 G_0. The plateau at 0.5 G_0 is the spin resolved plateau where the spin-degeneracy has been removed without an applied magnetic field. The 0.25 G_0 plateau has been seen in GaAs channels and has been identified [60] as a fully spin-polarised uni-directional current. The 0.25 appearance is symmetric unlike what we have observed in $In_{0.75}Ga_{0.25}As$ channels in Chapter 5. Figure 6.12 shows the transconductance dG/dV_{sg} plotted against source drain bias V_{sd} at B=0. Regions of bright grey correspond to a large amplitude of dG/dV_{sg} indicating the locations of subband transitions. This is useful along with figure 6.9b to to obtain the subband energy and the energy difference between spin split energy levels defined by the Zeeman energy E_z. We will use this to

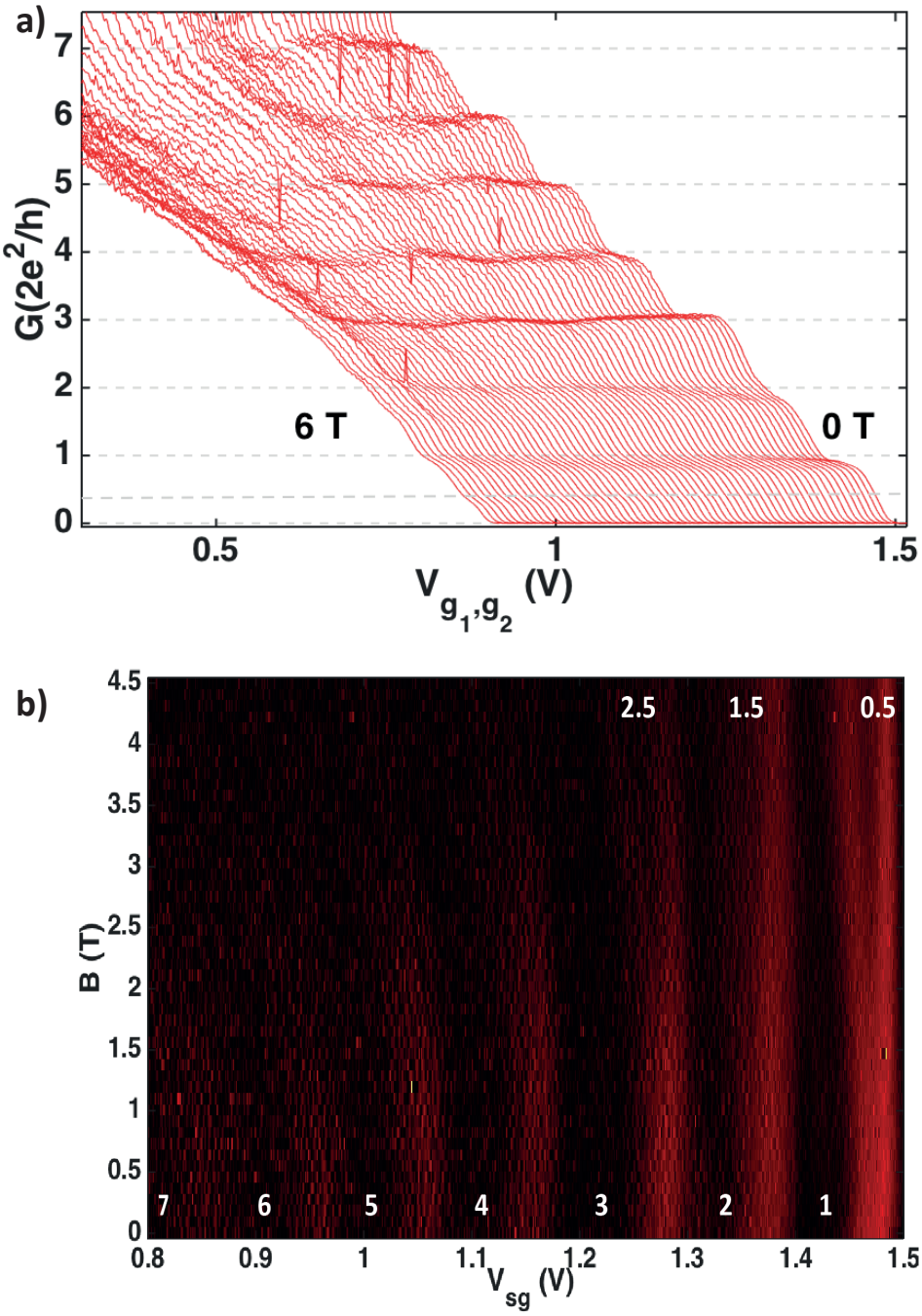

Figure 6.9: **a)**The differential conductance as a function of patterned gate voltage with B in-plane from 0 to 6 T in steps of 0.1 T. The top gate voltage V_{g3} was at 0V. **b)** Transconductance dG/dV_g as a function of split gate voltage V_{g1-g2} and magnetic field $B_{\|}$. Regions of light red indicate a large amplitude of dG/dV_g corresponding to locations of subband transitions.

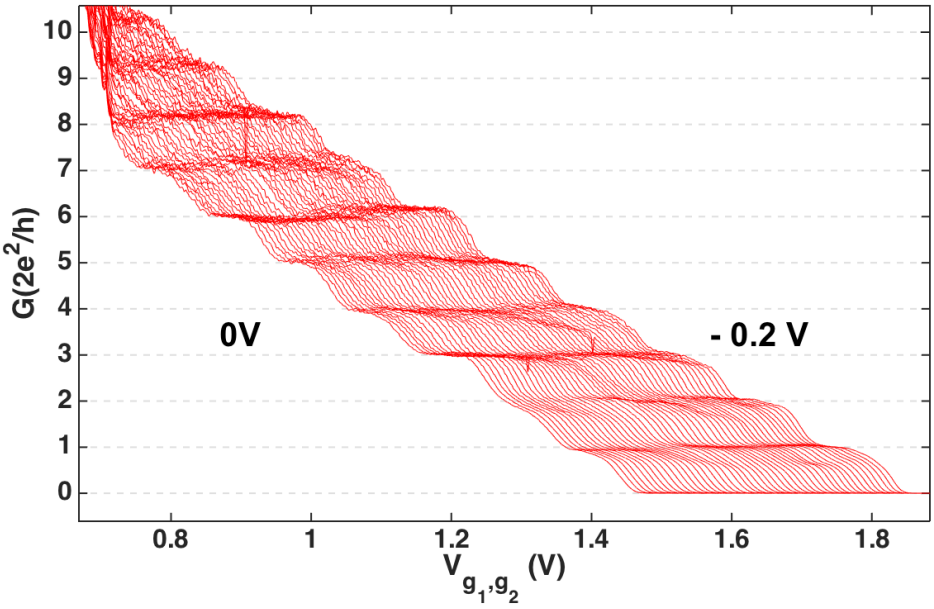

Figure 6.10: The differential conductance as a function of patterned gate voltage at 20 mK in enhancement mode. The global top gate voltage is stepped in -10 mV increments from 0 to -0.2 V (extreme right trace).

obtain a rough estimate of the g-factor in these systems providing a good comparison to $In_{0.75}Ga_{0.25}As$ system. Using the method introduced in chapter 4 we can obtain the g-factor. The subband separations $\epsilon_{n+1} - \epsilon_n$ are extracted from the main diamond structure by reading off the value V_{sd} where the straight light gray line surrounding the G=n diamond intersect, indicating the appearance of the next subband. For the first subband $\epsilon_{n+1} - \epsilon_n$ =0.6 meV. Using these figures along with $\delta V_g/\delta B_{||} = 0.036 \pm 0.02$ and $e\delta V_{sd}/\delta V_g$ of 8.5 (meV/V), the calculated g factor for the first subband is 5.1 $\pm$0.2. This is significantly lower than the g factor obtained for $In_{0.75}Ga_{0.25}As$ devices measured in this project. However it is still not consistent with the enhancement of g-factor seen in 1D regions [83], similar to $In_{0.75}Ga_{0.25}As$ devices (see chapter 5). The g-factor for the 2DHG in 2D was measured to be -4 to -7 [108, 109].

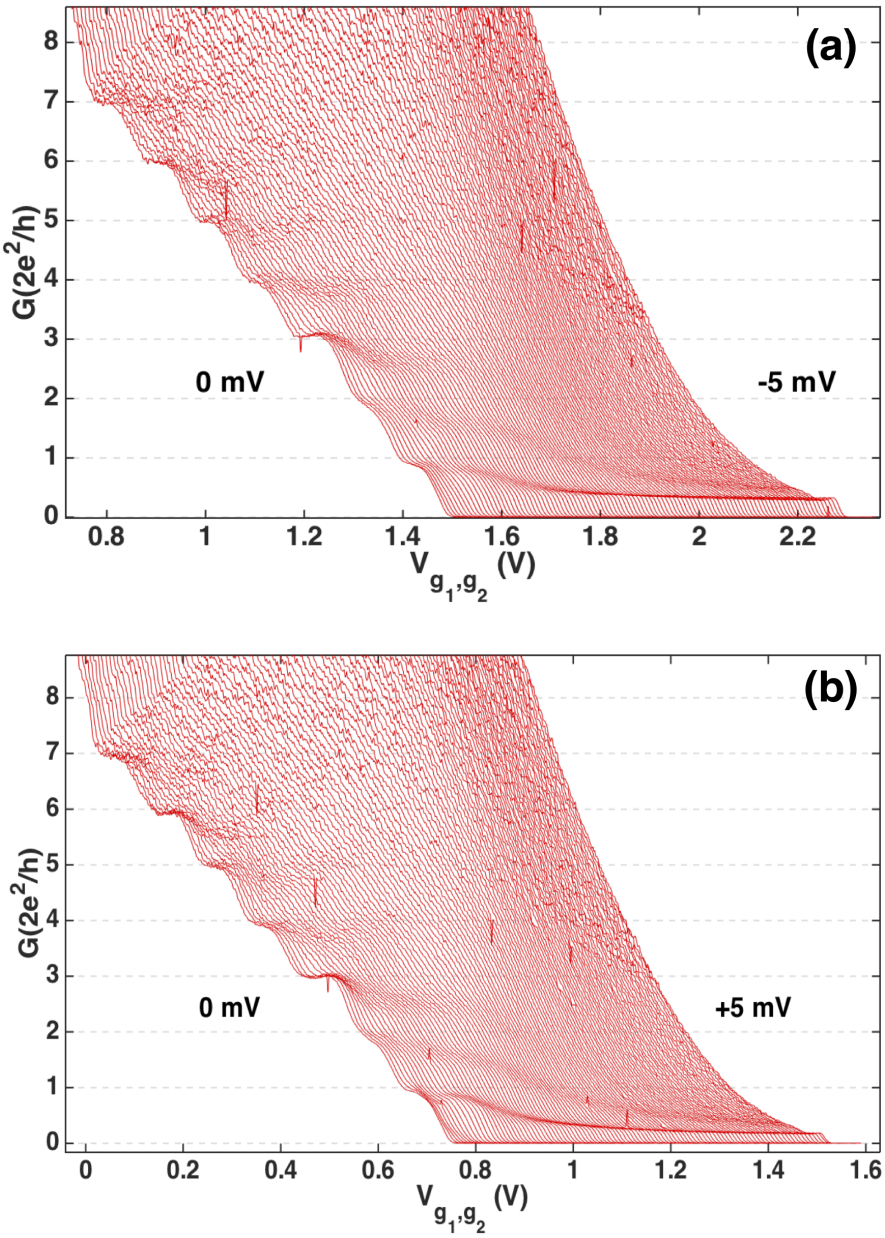

Figure 6.11: The differential conductance as a function of patterned gate voltage at 20 mK with $Vg_3 = 0$V. In (a) a dc source-drain bias is added from 0 to -5 mV in steps of -50 μV. In (b) a dc source-drain bias is added from 0 to 5 mV in steps of 50 μV.

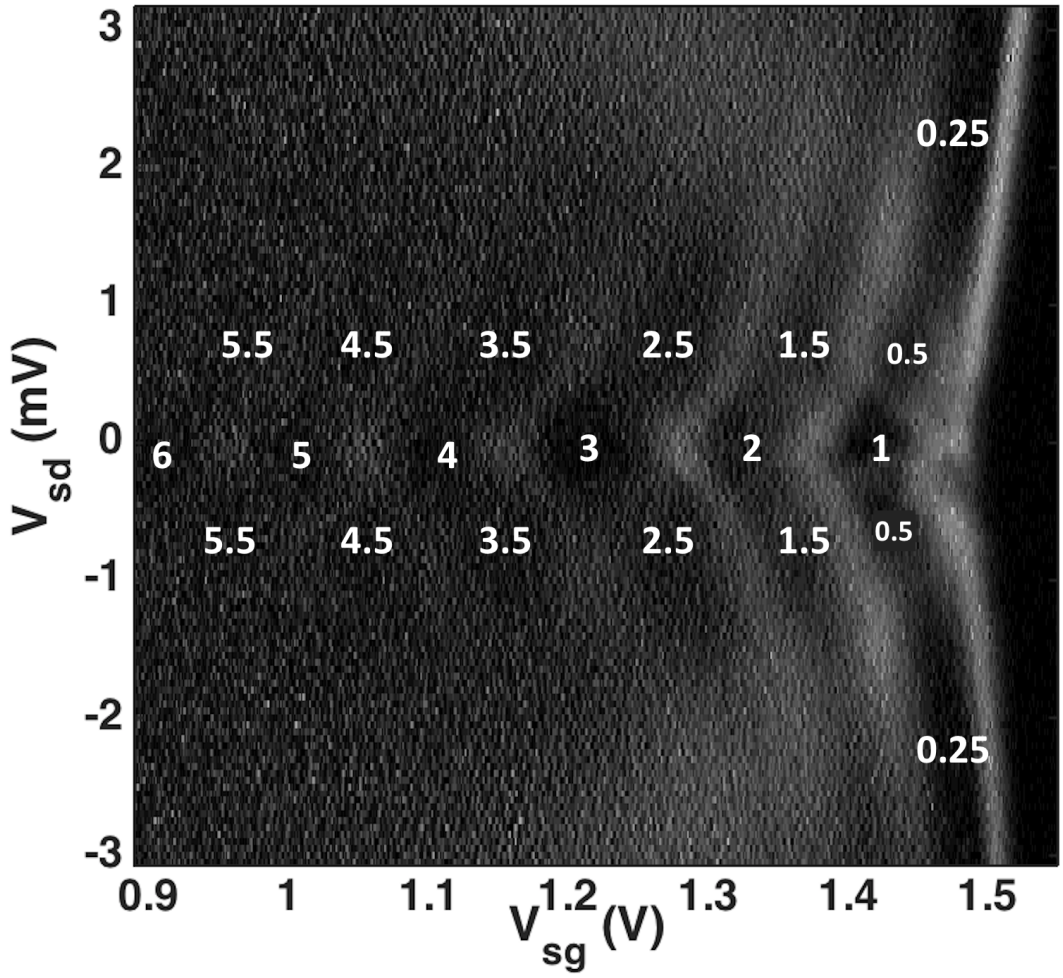

Figure 6.12: Transconductance dG/dV$_{sg}$ plotted against source-drain bias V$_{sd}$ at B=0. Regions of light gray correspond to a large amplitude of dG/dV_{sg}, indicating the locations of subband transitions.

6.5 Lateral bias

At $V_{g3} = 0$, the left hand trace of fig. 6.10 an asymmetric bias ($\Delta V = V_{g1}$-V_{g2}) to gates g1 and g2 was applied and is shown in fig. 6.13. This has the effect of laterally shifting the 1-dimensional channel between the surface gates g1 and g2. As fig. 6.13 shows, the integer conductance plateaus are robust and insensitive to the lateral shift. Extra features do occur such as the 0.5 G_0 structure as discussed earlier which moves towards the 0.7 G_0 (right hand side of 6.13. For some combinations of V_{g1} and V_{g2} double jumps can be seen in the conductance. This could be a manifestation of a re-ordering of the ground state into double rows [110] of charge p with G appearing as 2 G_0. This scenario is likely to be observed in high mobility structures and is a further good indication of the quality of the p-Ge hole gases reported in this work. A lateral spin-orbit coupling effect is not observed in this case.

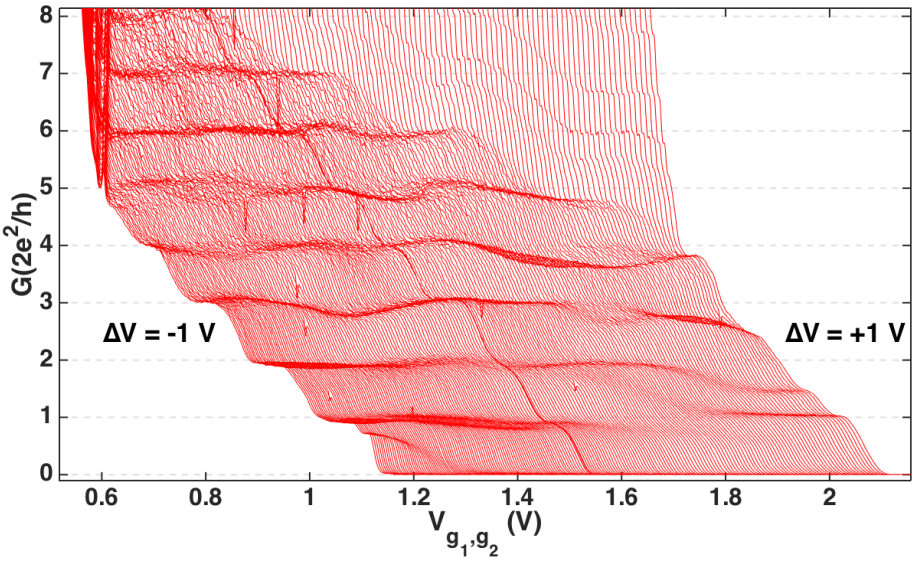

Figure 6.13: Asymmetric bias (with $V_{g1} \neq V_{g2}$) to the patterned gated up to V_{g1}-V_{g2} (labelled as ΔV) = $\pm$1 V at 20 mK in increments of ΔV= 10 mV. For all traces V_{g3} = 0 V. The thick line pinching off at 1.54 V is the case for ΔV= 0.

6.6 Summary

The observation of heavy hole spin splitting in the ballistic conductance of p-Ge was predicted in ref. [103] and is confirmed here up to 10 G_0. This project has laid the ground work for understanding the heavy hole spin splitting in p-Ge in 1-dimension considering that the angular momentum vector J is confined along the growth direction. Applied source-drain voltages and symmetric gating of the channel has uncovered plateau at half integer values as well as ballistic structure down to 0.25 G_0. The transport measurements carried out here have given a very good comparison to the $In_{0.75}Ga_{025}As$ wafers studied in this work.

In the next chapter we will analyse the 0.25 G_0 structure seen in the transport measurements carried out on p-Ge at low carrier concentrations and the many-body interaction effects seen in asymmetric split-gate bias measurements.

Chapter 7

Many body effects in Ge

7.1 Introduction

Chapter 6 provided us with a summary of characteristics of 1D transport in p-Ge system. The measurements carried out on p-Ge were kept similar to those in $In_{0.75}Ga_{0.25}As$ to provide a good comparison and to understand the role played by spin-orbit coupling. We have seen that the hole transport at high carrier density and mobility provides quantised ballistic transport that is similar to what has been seen in GaAs and InGaAs. However observing many-body interaction effects in 1D systems using transport measurements is a considerable challenge. The differential conductance measurements with ideal contacts gives rise to universal quantised conductance given by $G=G_0=2e^2/h$, independent of interactions [111, 112]. What makes p-Ge very interesting is that using a top gate to control the carrier density, provides us with a mechanism to lift the spin-degeneracy without external magnetic fields. Using top gate to induce many body effects has already been proven in GaAs devices where, the ground state reorganises it self in a row formation [110], and plateaus appear at 2 G_0 intervals. In this chapter we analyse the anomalous structures seen in the transport measurements of p-Ge split gates, and investigate possible sources responsible for these structures.

7.2 Fractional Charge

The unit of charge in nature is a fundamental constant, however the charge of individual quasi-particles in low-dimensional systems may be fractionalized. For a 1D system with momentum conservation, it is predicted that the charge of a unidirectional electron that is injected into the wire decomposes into right and left moving charge excitations carrying fractional charges $f_0 e$ and (1-f_0)e respectively [113, 114]. The charge fraction f_0 is given by

$$f_0 = \frac{(1 + g_c)}{2} \tag{7.1}$$

where g_c is the Luttinger-liquid interaction parameter, $g_c = v_F/v_c$, for a Galilean invariant system, where v_F is the Fermi velocity and v_c is the velocity of charge excitations. Approximately, $g_c \approx (1 + U/2\epsilon_F)^{-1/2}$, where U is the Coulomb interaction energy and ϵ_F is the Fermi energy. For non-interacting electrons f_0 approaches unity, and it is < 1 for repulsive interactions [115]. Previously shot-noise measurements have been used in detecting fractional charge in 2D systems [116, 117]. At frequencies exceeding $v_F/g_c L \sim 10^{10}$ Hz, where the excitation wavelength is shorter than the wire segment, noise and conductance data should reveal interaction effects [118, 119], however it is difficult to setup these measurements at low temperatures.

Angle-resolved photo-emission spectroscopy measurements on stripe-ordered cuprate materials provided the initial experimental indication of electron fractionalisation in one dimension [120]. Theoretical proposals to measure the fractional charge, include multi-terminal geometries, including a four-probe geometry, measuring voltage shot noise due to an impurity [121]. Measuring the suppression of Aharonov-Bohm interference between two weakly coupled wires is another method [122].

7.3 0.25 G_0 structure

The p-Ge system offers a system in which to study many body effects in 1 dimension. We have observed ballistic structure at 0.25 G_0 with a top gate on all the devices that have been fabricated and measured, when the hole density is reduced. This eliminates the possibility that the structure arises from an impurity site. From figure 6.8 we can see that a plateau near 0.25 G_0 appears when the top gate is $\sim$ 0.18 V. This can also be seen in figure 6.7a. The structure stays there until the channel becomes quasi-ballistic due to very low carrier densities and Coulomb blockade structures start to dominate. This is clearly seen in a false colour plot (see fig. 7.1). The figure shows

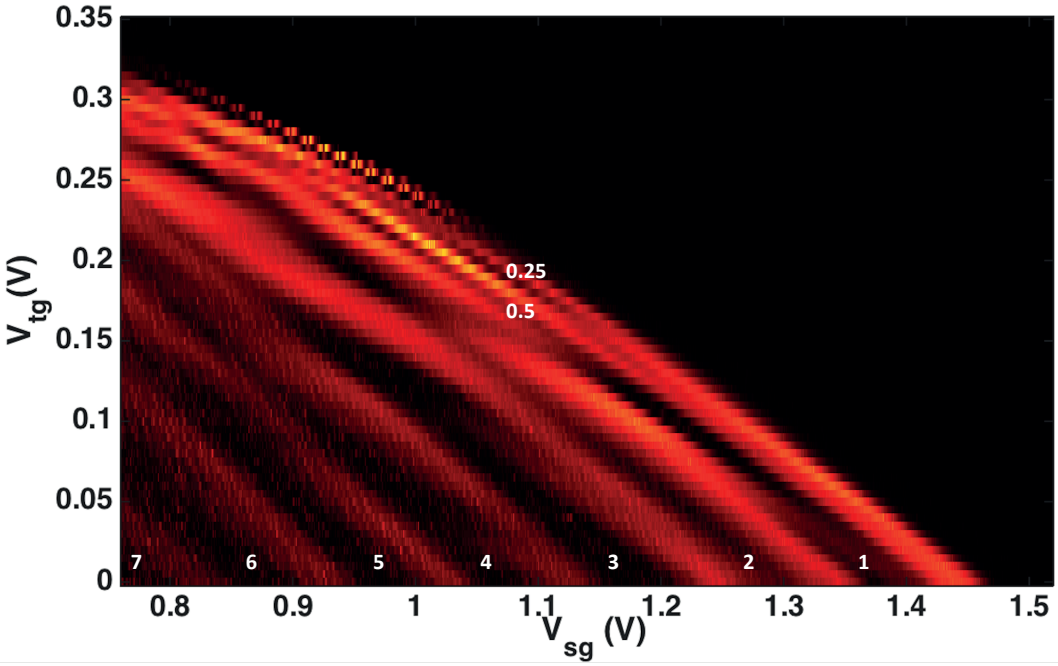

Figure 7.1: Transconductance dG/dV_g plotted against topgate voltage V_{tg} at B=0. Regions of light orange correspond to a large amplitude of dG/dV_{sg}, indicating the locations of subband transitions.

transconductance dG/dV_{sg} plotted against topgate voltage V_{tg} at B=0. Regions of light orange correspond to a large amplitude of dG/dV_{sg}, indicating the locations of subband transitions. The plateau at 0.25 G_0, is different to the fully spin polarised system seen in the non-ohmic regime, with an added d.c bias to source and drain (see fig. 6.11). In the case when a ferromagnetic order is formed only a 0.25 G_0 is seen [60]. This is explained as a fully spin polarised system that does not half in the presence of an in-plane magnetic field to 0.125 ($2e^2/h$) as it is already fully spin polarised. However in this case the other plateaux are still visible.

Applying an in-plane magnetic field causes the 0.25 G_0 plateau observed here to further half into 0.125 G_0 structure. Figure 7.2 shows the differential conductance as a function of split gate voltage, with V_{g3} held at 0.18 V, and the magnetic field is increased by 0.1 T intervals to 6 T. From the figure we can see the appearance of 0.125 G_0 structure, as the field is increased.

Applying a d.c. bias to the source-drain, causes the 0.25 G_0 structure to disappear rapidly with small d.c. voltage (> 0.5 V). The fully spin polarised state at 0.25 G_0 then appears for $V_{dc} > 2$ mV. This is shown in figure 7.3, which shows the differential

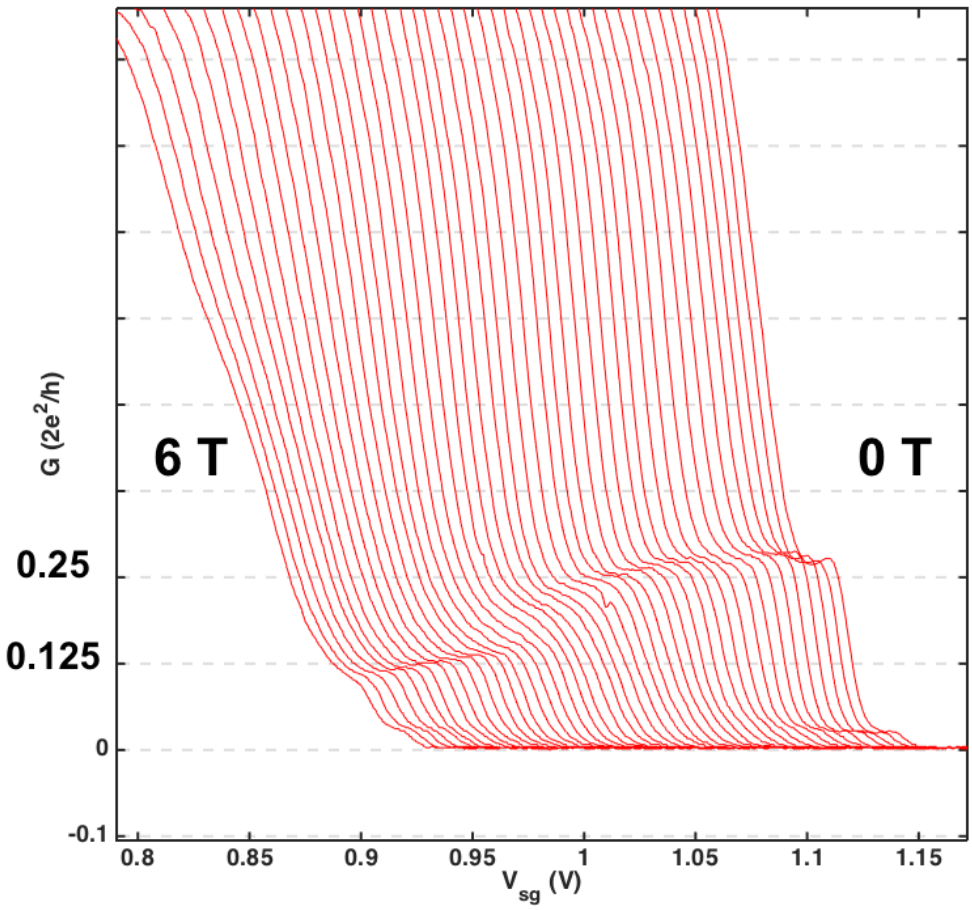

Figure 7.2: Plot of differential conductance as a function of split gate voltage (V_{g3} held at 0.18 V). The in-plane B-field is stepped up by 0.2 T. Data has been offset horizontally for clarity.

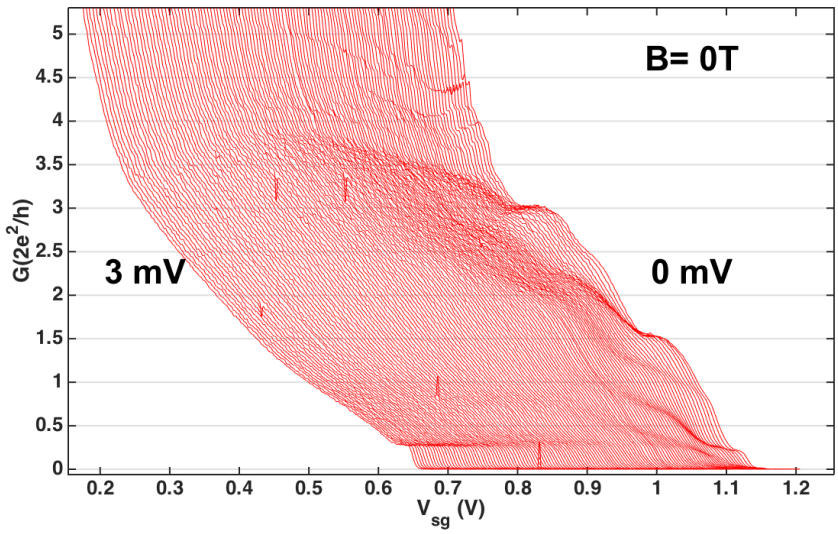

Figure 7.3: The differential conductance as a function of patterned gate voltage at 20 mK with $Vg_3 = 0.18$ V, with d.c source-drain bias added from 0 to 3 mV in steps of 50 μV. Data has been offset horizontally for clarity.

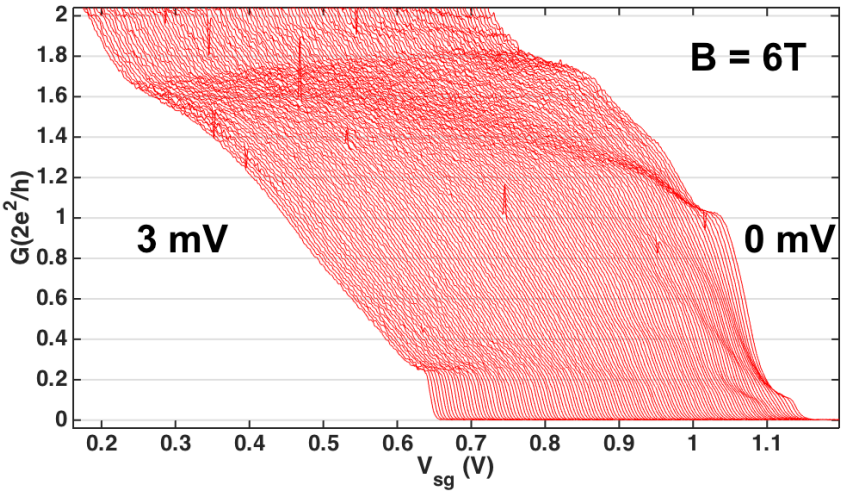

Figure 7.4: The differential conductance as a function of patterned gate voltage at 20 mK with $Vg_3 = 0.18$ V and an in-plane magnetic field B= 6 T, with d.c source-drain bias added from 0 to 3 mV in steps of 50 μV. Data has been offset horizontally for clarity.

conductance as a function of patterned gate voltage at 20 mK with $Vg_3 = +0.18$ V, with a d.c. source-drain bias added from 0 to 3 mV in steps of 50 μV. We have repeated this measurement with an in-plane magnetic field of B = 6 T, this is when we see the 0.125 G_0 structure at $V_{sd} = 0$ mV. As seen in the case of the 0.25 G_0 structure, the 0.125 G_0 structure disappears rapidly with small d.c bias on source-drain. Figure 7.4 shows the differential conductance as a function of patterned gate voltage at 20 mK with $Vg_3 = +0.18$ V with a 6 T in-plane magnetic field, with a d.c. source-drain bias is added from 0 to 3 mV in steps of 50 μV. This feature could be explained to be a 'soliton' [123]. The soliton is destroyed with finite source-drain voltage to be replaced by a spin-polarised 1-D hole gas at 0.25 ($2e^2/h$).

7.4 Possible explanations

7.4.1 Solitons

The Su-Schrieffer-Heeger (SSH) model[123, 124] may provide an explanation for the observed structures. The SSH model describes a one-dimensional chain, characterised by two tunnelling amplitudes t_1 and t_2 between two sublattices A and B. It provides a model for studying fractionalized charges, if interfaces exist in the lattice potential to separate topologically distinct chains into multiple domains in the real space [125, 126]. To model the SSH a double-well optical lattice has been shown to be a powerful tool [127, 128]. A possible explanation for the emergence of the 0.25 G_0 structure could be that holes in Ge forms pairs with neighbouring holes, forming a symmetric ground and an anti-symmetric first excited state. In the ground state the two holes are coupled so move together or else some complex motion which involves pairs constantly reforming and breaking. Considering on-site repulsive interaction, the potential,

$$\hat{V} = U \sum_j (\hat{n}_{j,a\uparrow}\hat{n}_{j,a\downarrow} + \hat{n}_{j,b\uparrow}\hat{n}_{j,b\downarrow}) \tag{7.2}$$

where U$>$ 0 is the on-site interaction strength, j is the site index of the double-well lattice, $\uparrow, \downarrow$ are the spin up and spin down, respectively. Flatbands arise in the extreme case when $t_2 = t_1 = 0$. In this case localised orbitals $\hat{c}^\dagger_{j\uparrow}|0\rangle = (\hat{a}^\dagger_{j\uparrow} + \hat{b}^\dagger_{j\uparrow})|0\rangle/\sqrt{2}$ and $\hat{c}^\dagger_{j\downarrow}|0\rangle = (\hat{a}^\dagger_{j\downarrow} + \hat{b}^\dagger_{j\downarrow})|0\rangle/\sqrt{2}$ are degenerate eigenstates of this flatband with energy t_1. Where $\hat{a}$ and $\hat{b}$ are the creation operators for spin-up or spin-down atoms at the left and right wells on site j. In this case a ferromagnet emerges at half filling and all electrons/holes fill up either spin up or spin-down chain. This is illustrated in fig. 7.5.

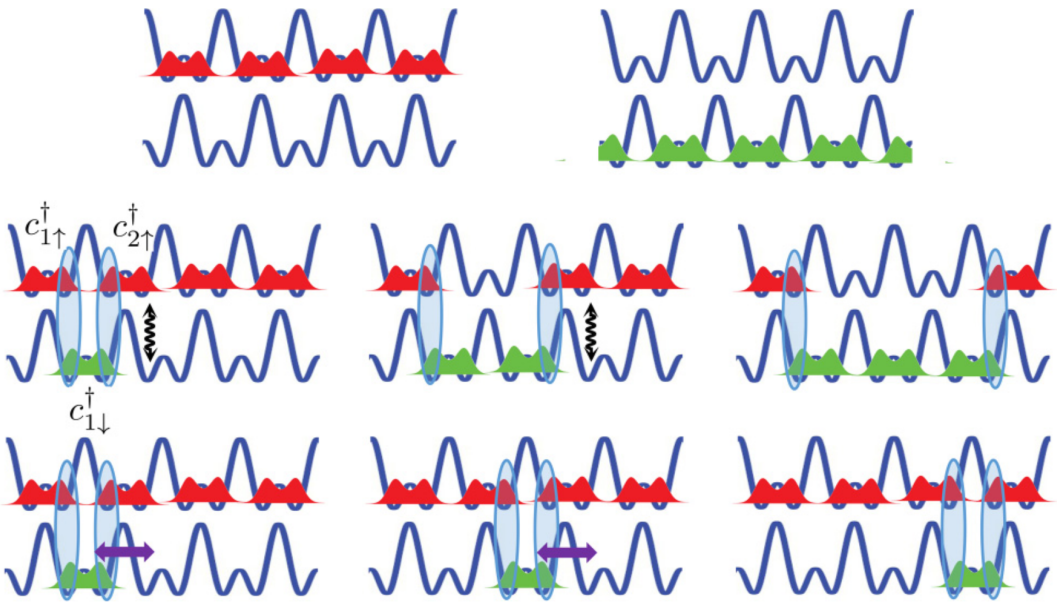

Figure 7.5: Charge fractionalization. *top)*At half-filling, a repulsive interaction leads to spontaneous symmetry breaking and a ferromagnet emerges. The red and green clouds represent the Wannier wave functions of the spin-up and spin-down particles, respectively. *middle* Doping an extra particle forms two domain walls (blue ovals). If $t_2 = 0$, the two domain walls are de-confined because of interchain tunneling t (black wiggle). *bottom)* If $t = 0$, the two domain walls are confined for any finite interchain tunneling t_2 (purple arrow). Figure adapted form ref. [124].

This state saves energy and does not cost extra kinetic energy. This means a repulsive interaction lifts the single-particle degeneracy, resulting in a ferromagnet with a twofold degeneracy, and the ground state can be $|G\rangle_1 = \prod_j \hat{c}^\dagger_{j\uparrow}|0\rangle$ or $|G\rangle_2 = \prod_j \hat{c}^\dagger_{j\downarrow}|0\rangle$. If this is the case then in a degenerate ferromagnet state when we apply an in-plane magnetic field this degeneracy lifts and hence we get the 0.125 G_0 structure. This is a highly speculative explanation and further measurements along with theoretical models would help with the explanation. For more details on the SSH model please see references [123, 124, 125, 126].

When the source-drain voltage is increased this has the effect of breaking the pairing so there is a transition to single electron behaviour which means that the conductances are increased by a factor of 2 as pairing is eliminated.

We can obtain the energy loss due to the pairing, when we plot the transconductance

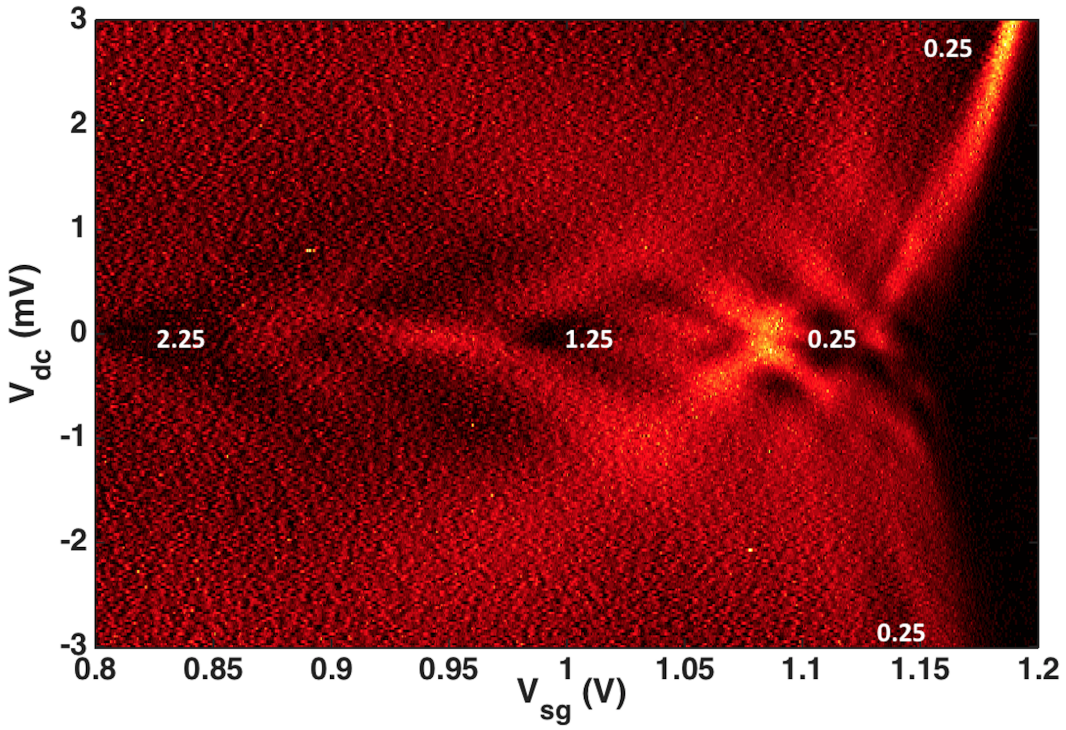

Figure 7.6: Transconductance dG/dV$_{sg}$ plotted against d.c bias V$_{dc}$ at B=0. Regions of light orange correspond to a large amplitude of dG/dV_g, indicating the locations of subband transitions.

dG/dV$_{sg}$ against source drain bias at B=0 T. The regions of light orange correspond to a large amplitude of dG/dV_{sg}, and indicate the locations of the subband transitions. This is shown in figure 7.6. From the figure we can determine the energy loss due to the pairing, which is $\sim$ 0.25 meV.

Temperature dependence measurements have shown that both 0.25 G$_0$ and 0.125 G$_0$ are robust up to $\sim$ 1 K. Figure 7.7 shows differential conductance as a function of split gate voltage at 20 mK and 1 K. From the figure we can see that the 0.25 G$_0$ structure is stronger at 20 mK and we can still see it at 1 K. Similar to 0.25 G$_0$ structure the 0.125 G$_0$ structure is robust to temperatures up to $\sim$ 1 K. Figure 7.8 shows the differential conductance as a function of split gate voltage at 20 mK and 900 mK at B = 6 T.

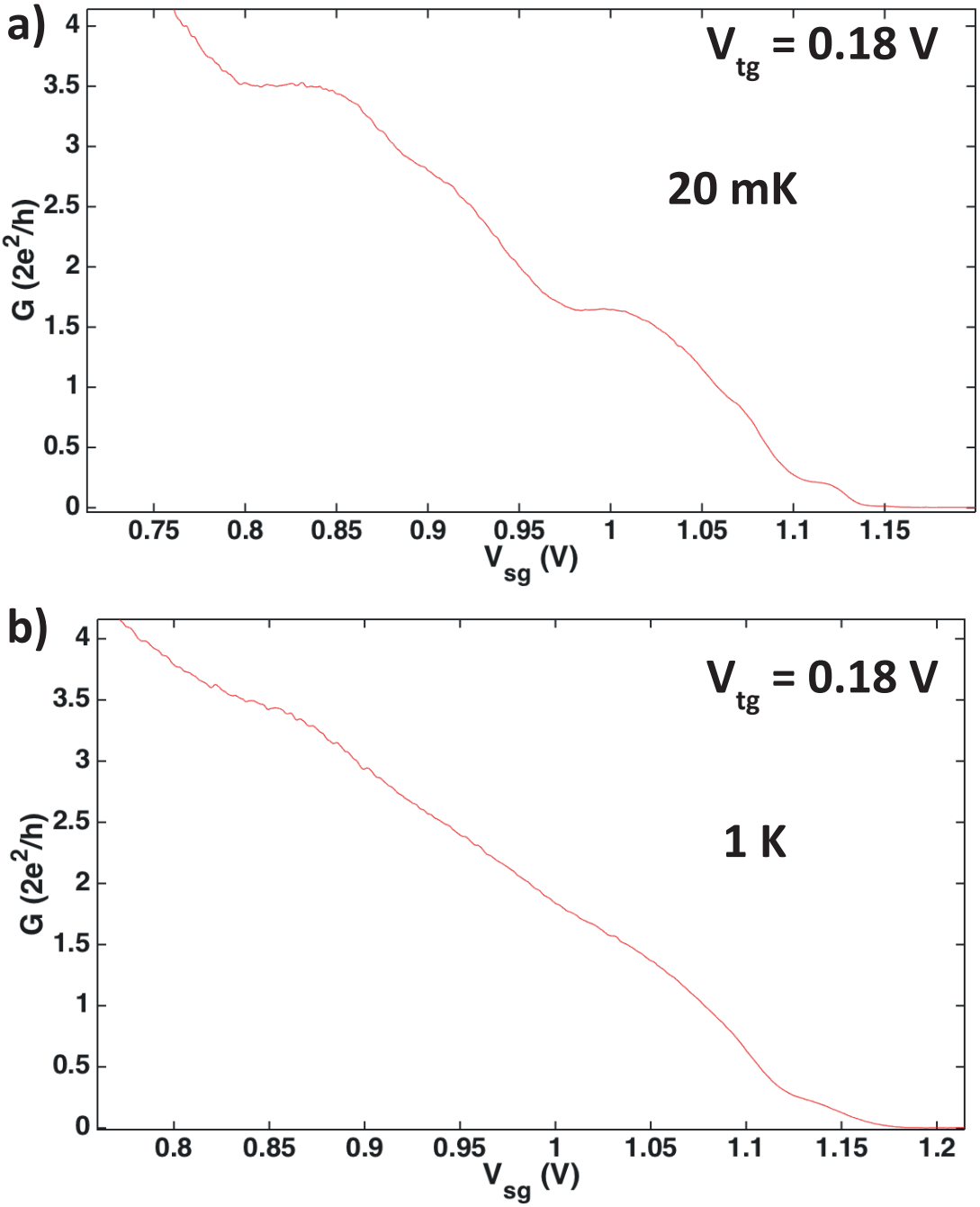

Figure 7.7: Differential conductance as a function of split gate voltage at 20 mK **(a)** and 1 K **(b)** at B = 0 T, and V_{g3} = 0.18 V.

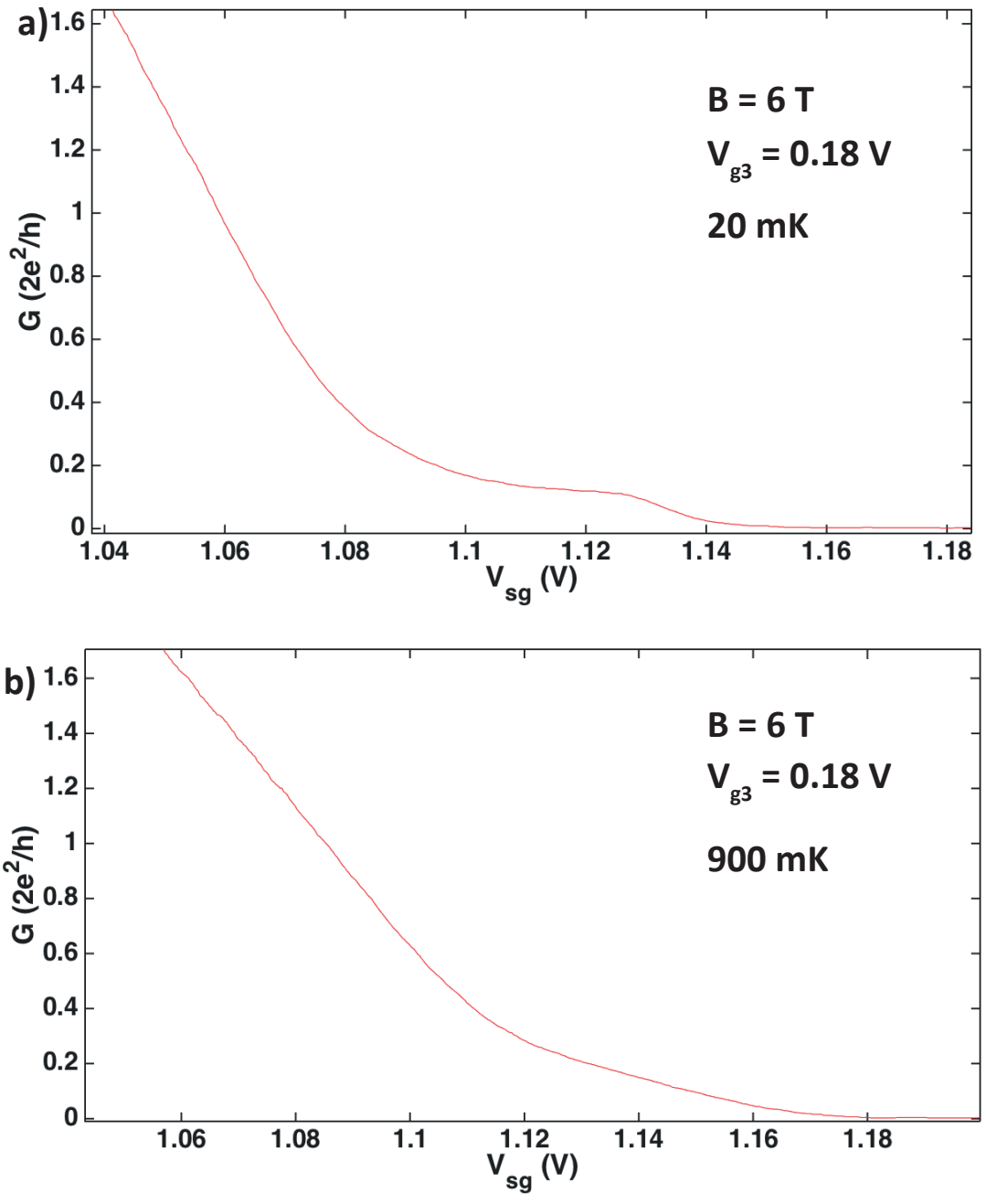

Figure 7.8: Differential conductance as a function of split gate voltage at 20 mK **(a)** and 900 mK **(b)** at B = 6 T, and $V_{g3} = 0.18$ V.

7.4.2 Fractional Wigner Crystal

The Luttinger liquid, describing low energy gapless one dimensional systems can provide another explanation [129, 130]. In reference [131] it was proved that the Fermi operator $\Psi_s(x)$, where s $=\pm$ is the spin projection, of a generic one dimensional electron system can be very different with respect to the Luttinger model [131, 132]. In the standard relation

$$\psi_s \sim e^{i\theta(x)} \sum_{p=\pm 1} e^{-ipk_F x} e^{ip\phi(x)} \tag{7.3}$$

where k_F the Fermi momentum and $\phi(x)$ and $\theta(x)$ the usual bosonic fields, is replaced by a more general expression.

$$\psi_s \sim e^{i\theta(x)} \sum_{p=-\infty}^{\infty} c_p^{(s)} e^{-ipk_F x} e^{ip\phi(x)} \tag{7.4}$$

where $c_p^{(s)}$ is the model dependent coefficients. A model has been developed in reference [133] for a strongly interacting Helical Luttinger liquid [134, 135], when the spin-momentum locking breaks the symmetry $c_{-p}^{(s)} = c_p^{(s)}$. Reference [133] develops a strongly interacting Luttinger liquid quantum spin Hall system in the presence of two-particle backscattering extending over the full helical edge. This system is characterised by charge oscillations which are half the wavelength of the usual Wigner crystal, which suggests the formation of a correlated state of fermions with charge $e/2$, with e the electron charge. This can be visualised by two-particle backscattering bringing two-particles from one branch of the dispersion relation to the other one, and there is a momentum transfer of $4k_F$. From Landau's theory of the Fermi liquid, the helical liquid in the presence of two-particle backscattering can be reformulated in terms of new quasi-particles. In the presence of strong interactions (Luttinger parameter $K_L < 1/2$, where $K_L = \nu_F/\nu$), two-particle backscattering becomes relevant, and determines the nature of the quasi-particles. The two-particle backscattering can be viewed as a single quasi-particle backscattering term, thus the Femi momentum k'_F of the quasi-particles becomes $2k'_F$. As there are two quasi-particles, their charge becomes e/2 because of charge conservation. For a more thorough explanation please see reference [133].

7.5 Wigner Crystal

Electronic properties can be altered by the modification of the confinement potential, for example by inducing a reflection at the channel exit, the system can display Kondo behaviour [136]. Recent works have shown that when the confinement is weak, the ground state conduction is $2G_0$ ($4e^2/h$) [137, 138, 139]. The splitting was linked to the splitting of electrons in the ground state into two separate rows, each with conductance of G_0. These row formation has the lowest energy state which minimises the electron-electron interaction, as a result of weakening of the confining harmonic oscillator potential. This is the incipient Wigner lattice where the electrons form a 'zigzag' configuration, and upon configuring the confining potential with the means of a topgate [110] or a asymmetric split gate [139] leads the electrons to separate into two rows [140, 141, 142].

The confinement potential can be altered by applying a lateral bias to the split gates. The asymmetric lateral confining potential has been shown to induce spin polarisation in InAs QPC devices [39]. In our devices when we induce asymmetric lateral confining potential we have not observed the spin polarised 0.5 G_0 structure. However for some combinations of V_{g1} and V_{g2} double jumps can be seen in the conductance. This could be a manifestation of a re- ordering of the ground state into double rows of charge [p] with G appearing as 2 G_0. Figure 7.9 shows the asymmetric split-gate biasing (with $V_{g1} \neq V_{g2}$) to the patterned gated up to V_{g1}-V_{g2} (labelled as ΔV) = + 1.6 V at 20 mK in increments of ΔV= 10 mV. From the figure we could see that at Δ V $\sim$ 0.8 V, we see that the plateau at G_0 weakens and 2 G_0 becomes the ground state. The plateau at G_0 reappears as the lateral bias is increased but along with a plateau at 1.5 G_0. Figure 7.10 is the grayscale plot of transconductance (dG/dV_{sg}) as a function of V_{sg} and ΔV. Although weak you can see an anticrossing (white dotted circles) of the subbands around Δ V $\sim$ 0.8 V, corresponding to double-row formation.

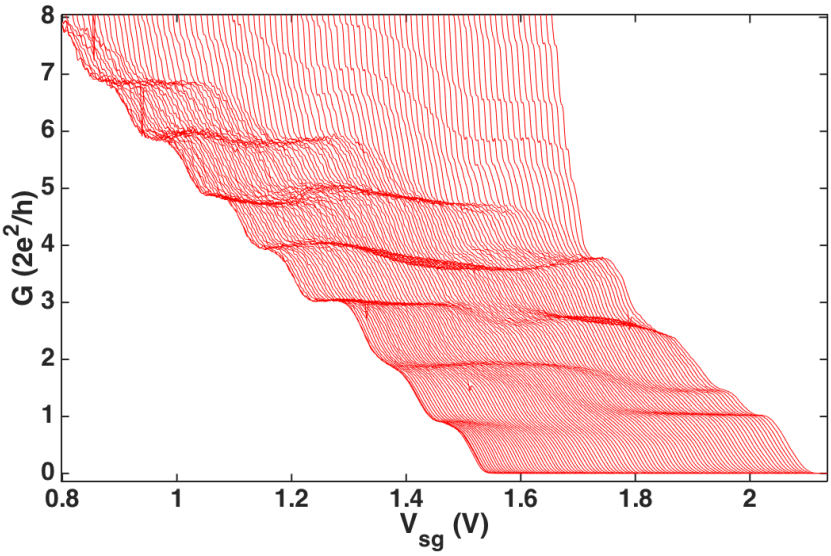

Figure 7.9: Asymmetric bias (with $V_{g1} \neq V_{g2}$) to the patterned gated up to V_{g1}-V_{g2} (labelled as ΔV) = + 1.6 V at 20 mK in increments of ΔV= 10 mV. For all traces V_{g3} = 0 V. The extreme left line pinching off at 1.54 V is the case for ΔV= 0.

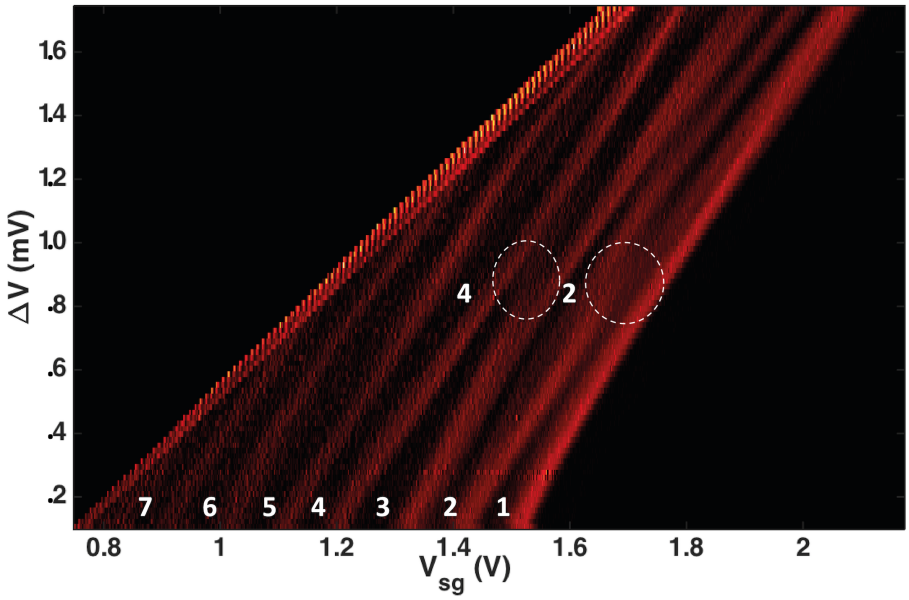

Figure 7.10: Transconductance dG/dV_{sg} plotted against lateral bias ΔV at B=0. Regions of light orange correspond to a large amplitude of dG/dV_{sg}, indicating the locations of subband transitions. The anti-crossings are highlighted by white dotted circle.

7.6 Summary

The p-type Ge system provided us with a very good platform to study many body effects. The observation of 0.25 G_0 structure along with 0.125 G_0 structure demonstrates that many body effects are strong in p-Ge. However more measurements, and measurements with higher mobility, low carrier concentration samples would give a more clearer picture of the physics of hole transport in these systems, along with a in-depth theoretical work. The system can be further studied along with the role played by the compressive strain and control of the light hole contribution can be understood in Ge for p-MOS, fundamental spintronic devices and Majorana fermion studies. In this chapter we have introduced fractional charge as a candidate for the appearance of the 0.25 G_0, although this is a highly speculative explanation. Fractional quantisation arising from fractional charge, in the absence of a quantising magnetic field, has been proposed for different experimental situations, commencing with the Su-Schrieffer-Heeger model [123, 126] of an e/2 domain wall propagation due to a defect between two degenerate phases of polyacetylene dimer. However, as the domain wall boundaries come in pairs the resultant charge is unity rather than fractional, such features in this material were not observed due to a high level of disorder. Other predictions are based around a Mott Insulator or domain boundary between two topological phases in 1D [143]. It has been shown that there is a measurable 2D S-O interaction in the Ge utilised here but it is of Rashba type [95] induced by a negative gate voltage and higher carrier concentration than used in the work reported here. In our device scheme we have used a positive top-gate voltage to deplete the carriers and achieve a 2D carrier concentration of 1010 cm^{-2} which is necessary for observation of the fractions.

The next chapter will summarise the future work that will be carried out on $In_{0.75}Ga_{0.25}As$ and p-Ge devices.

Chapter 8

Progress and Future work

This project has explored two distinct systems that can be used for future spintronic devices. In this project we have measured the electron transport properties of $In_{0.75}Ga_{0.25}As$ heterojunctions, and determined how Rasha spin orbit coupling effects the ballistic transport. It was shown that ballistic transport through $In_{0.75}Ga_{0.25}As$ split gated devices show similar transport properties to GaAs devices. However Rashba SOI reduces the magnetic field needed to lift the spin degeneracy. We have also determined the g factor of the $In_{0.75}Ga_{0.25}As$ in 1D to be 6.5.

In this project we have also introduced the p-Ge system, and explored the 1D transport properties in these systems. The p-Ge system is very different to the $In_{0.75}Ga_{0.25}As$, as there was no Rashba spin orbit coupling in 1D. However low carrier densities along with compressive strain provided us with a system where the hole spin can be altered without external magnetic fields.

The main objective of this project was to explore spin-dependent transport in semiconductor nanostructures. The materials chosen for this project included two completely different systems, and by keeping the measurements similar to each other it has provided a good comparison, and have enabled us to investigate spin dependent transport in these systems. This project has also laid the ground work for creating more complex device geometries that can enable measurements to detect entanglement and provide a platform that could eventually aid quantum computation.

8.1 Summary of Results

We have successfully fabricated surface gated devices on both $In_{0.75}Ga_{0.25}As$ wafers and p-type Ge wafers. Using split-gate devices to define quantum wires in a (2DEG) or (2DHG) system is an effective way to study many-body effects driven by electron-electron or hole-hole interactions in a 1D constriction [4, 97]. The experiments reported in this thesis provide advances in 1D transport in $In_{0.75}Ga_{0.25}As$ wafers, and have laid the ground work for understanding the transport mechanisms of heavy holes in p-Ge.

The first experiments reported in chapter 4, provided a summary of previous work carried out on InGaAs, and summarised the results obtained on low mobility $In_{0.75}Ga_{0.25}As$ wafers, along with transport measurements carried out on high mobility wafers to optimise the fabrication methods and determine ideal length scales needed for clean ballistic channels.

Chapter 5 summarised the low temperature measurements carried out on high quality split gates fabricated on the W436 wafer. Previous studies in InGaAs systems required perpendicular magnetic field to reduce the disorder to observe quantised conductance [72, 76]. In this project we have optimised the fabrication methods and determined ideal length scales to observe clear ballistic plateaus. In this low disorder system no perpendicular magnetic field is needed to observe conductance plateaus at $2e^2/h$ intervals.

In $In_{0.75}Ga_{0.25}As$ a weaker backscattering due to the time-reversal asymmetry in the one-dimensional channel results in enhanced ballistic transport characteristics with clear quantised conductance plateaus up to $6(2e^2/h)$. Finite applied voltages between the source and drain contacts and the application of an in-plane magnetic field confirm this picture. For asymmetric patterned gate biasing, a lateral spin-orbit coupling effect is weak. However, the Rashba-type spin-orbit coupling leads to an anisotropic g-factor in the 1-dimensional channel that is reduced in magnitude from the 2-dimensional value of ~ 9 to 6.5 in the lowest subband when the effective Rashba field and the applied magnetic field are perpendicular.

In Chapter 6 we have introduced the Ge 2DHG system. In the 1D regime we have no Rashba field and SOI is limited in these systems as Dresselhaus spin-orbit interaction due to bulk inversion asymmetry is absent[32]. The effective mass of the heavy holes makes it comparable to electrons in GaAs. We have used high mobility Ge Hole gas systems grown at the University of Warwick to fabricate split gated devices. Chapter 6 has laid the ground work for understanding the heavy hole spin splitting in p-Ge in one-dimension considering that the angular momentum vector J is confined

along the growth direction. Applied source-drain voltages and symmetric gating of the channel has uncovered plateau at half integer values as well as ballistic structure down to 0.25 G_0. The transport measurements carried out here were kept similar to that of $In_{0.75}Ga_{0.25}As$ wafers and have given a very good comparison to the $In_{0.75}Ga_{025}As$ wafers studied in this project.

In Chapter 7 we have analysed the anomalous structures seen in the transport measurements in p-Ge, and investigated possible sources responsible for these structures. We have introduced Solitons and fractional Wigner crystal as a possible explanation for the 0.25 G_0 structure. However further studies are needed to fully understand the mechanisms behind this anomalous structure. We have also shown that we can alter the confining potential using lateral gate voltages to create a row formation as the ground state effectively creates a Wigner lattice. The hole-hole interaction strongly modifies the sequence of quantum levels in the Ge quantum wire created by the spatial confinement. When the confinement is relaxed so that the system can expand in the second dimension there is a disappearance of the ground state, (that has half sine character), and it is replacement by a more complex structure producing fractional quantisation with charges e/2 and e/4. This observation suggests a new area of experimentation in quasi one-dimensional systems, particularly direct measurement of the charge, with implications for possible schemes of topological quantum information processing [144]. The clarity of the new states observed in s-Ge will also provide enhanced understanding to conductance structure below the first ballistic plateau found with electrons in GaAs.

8.2 Future Work

For further work we will continue to fabricate split gates with top gates on high mobility p-type Ge and $In_{0.75}Ga_{0.25}As$ wafers. We will expand the work on fractional quantisation observed in this project and carry out experiments to see if we can observe fractional quantisation in other systems such as in holes in GaAs along with electrons. To confirm that the charge is fractionalised several measurements will be setup such as shot noise measurement to measure the charge [145]. Noise will be measured directly to determine the fractional charge value responsible for the conduction process. This requires the establishment of weak back-scattering when the shot noise is given by $S = 2QI_B$ where I_B is the backscattered current and Q is the charge.

The possibility that a zig-zag regime, which has been discussed theoretically, but not in the context of fractional charge, raises many possible scenarios of fractional

charges and complex spin states even a zero-spin excitation. For further work we will create interferometers and Aharonov-Bohm structures to study phase changes in the various fractional regimes. These devices can include quantum dots which will be of interest in determining whether fractions survive tunnelling and storage.

This project has laid the ground work needed for fabricating more complex devices on both $In_{0.75}Ga_{0.25}As$ and p-Ge. We have optimised the fabrication methods that are suitable for fabricating more complex devices. We have fabricated a series of devices that include single electron/hole quantum pumps, spin focusing devices and superconductor-semiconductor-superconductor hybrid devices in $In_{0.75}Ga_{0.25}As$ and p-Ge.

8.2.1 Quantum pumps

Quantum pumps on both $In_{0.75}Ga_{0.25}As$ and p-Ge wafers have been fabricated as a continuation of this project. These devices will be measured in a low noise measurement system. Figure 8.1 shows an SEM image of the quantum pump fabricated on p-Ge. This will be used to generate quantised current as a function of the frequency of an oscillating gate. Similar pumps were demonstrated in GaAs [146]. The two rightmost gates can be used as a pump, in our design there is a split gate at the exit. The blue arrow indicates the direction of the pumping. The pump can be operated by fixing one of the gates at a positive voltage to form a barrier, and the other gate will be modulated to pump the holes over that barrier. We will develop quantum pumps on both InGaAs and p-Ge to be used in an electron and hole interferometry experiment. For this we will incorporate the pump with an Aharonov-Bohm ring (AB-ring). When an electron/hole propagates around an AB-ring in the presence of a magnetic flux, it experiences a phase change. When electrons/holes travel through a narrow wire that splits into two channels; they have equal probability of travelling on either channels and then recombine as well as the wave function that also splits into two coherent partial wave functions that recombine when the wires meet. When there is an enclosed magnetic flux, the phase change experienced by these partial wave functions is different, and they will either combine constructively or destructively depending on the enclosed magnetic flux. Incorporating an AB-ring with two electrons or holes from a quantum pump, should enable us to detect entanglement schemes.

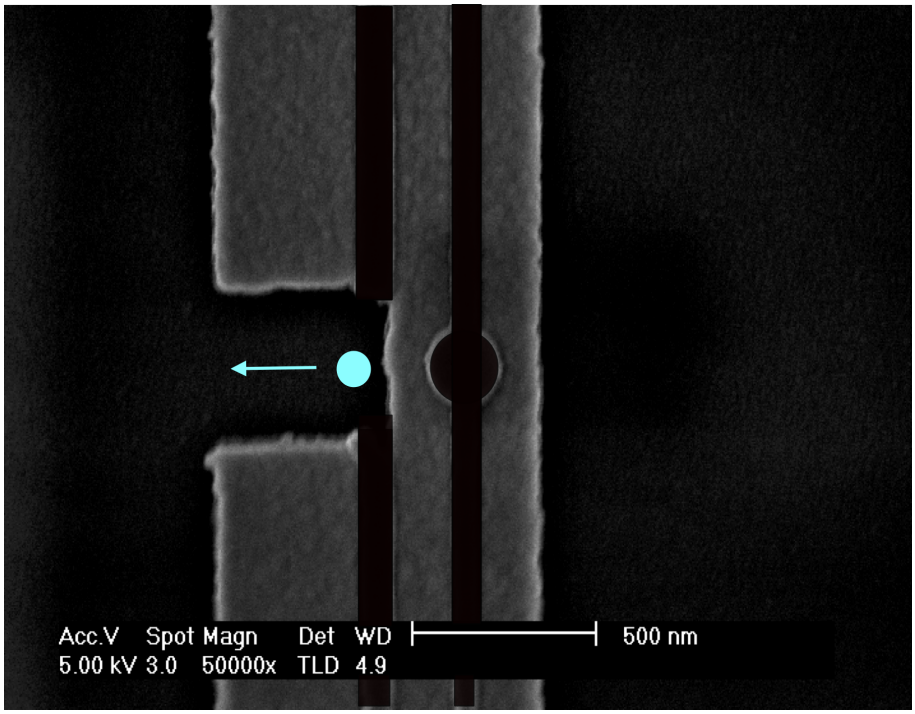

Figure 8.1: SEM image of quantum pump on p-Ge.

8.2.2 Focusing devices

Spin focussing has been demonstrated in both GaAs devices[147, 148, 149] and recently in InGaAs [150]. We have implemented this in p-Ge to focus spin polarised current in holes. The first step will be to demonstrate focussing in p-type Ge. Once the geometries and fabrication methods are optimised a more complex arrangement of gates can be utilised for on-chip spin manipulation for applications in spintronics and quantum information technology.

8.2.3 Superconductor-Semiconductor-Superconductor hybrid devices on InGaAs and Ge

There is a renewed interest in hybrid superconductor-semiconductor-superconductor (S-Sm-S) junctions and Andreev devices [151]. This is due to the recent reports of detections of Majorana fermions at the interfaces of these junctions [152]. A prerequisite for the Majorana fermion is a transmissive interface between a superconductor and 1-dimensional channel that has a large g-factor and spin-orbit interaction. We have started making these junctions on both $In_{0.75}Ga_{0.25}As$ and n and p-type Ge with transmissive Niobium superconducting contacts. The collaborative work has led to development of topological superconductivity based on hybrid Nb-$In_{0.75}Ga_{0.25}As$-Nb that that resulted in hard superconducting gap detection in symmetric, planar, and ballistic Josephson junctions [153].

Fig 8.2 shows an SEM image of one of the Nb contacted Ge devices. Initial measurements on these devices led to observation of an Andreev reflection effect between an s-wave superconductor and a germanium channel (see fig. 8.3). The coherence lengths are sufficiently long in the Ge to observe the effect up to 800 nm. The normal interface resistance contribution varies from 4.5 kOhm to 7 kOhm without a significant increase of the zero bias conductance ratio. We will also implement a split gate within these junctions to control the channel width.

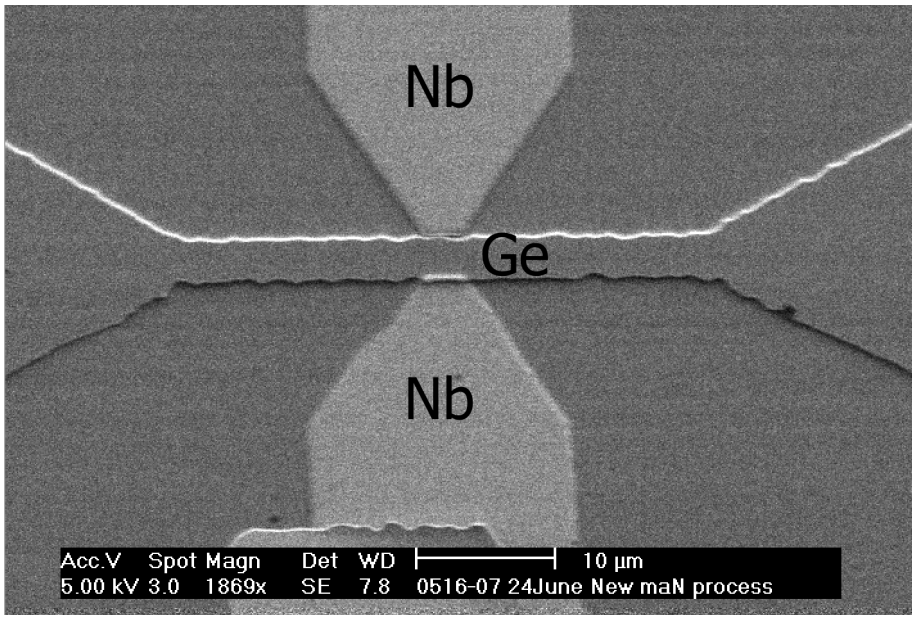

Figure 8.2: SEM image of Nb contacted Ge hall bar.

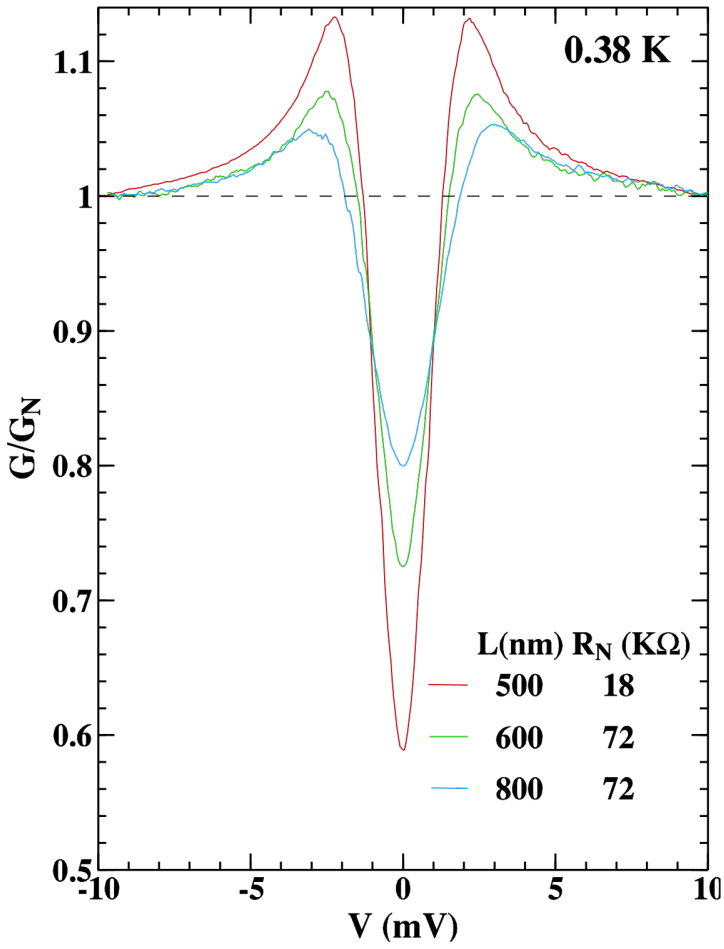

Figure 8.3: The differential conductance normalised to the normal conductance (G_N) in n-type Ge at 1.6 K as a function of dc bias voltage (V_{dc}) down to 500 nm gap.

8.3 Concluding Remarks

In this thesis we have explored two distinct material systems n–$In_{0.75}Ga_{0.25}As$ and p-Ge. The $In_{0.75}Ga_{0.25}As$ system has a high SOI due to the Rashba field. In these systems the effect of Rashba SOI provided us with a system that can be spin polarised with small magnetic fields. A weaker backscattering due to the time-reversal asymmetry in the 1-dimensional channel resulted in enhanced ballistic transport characteristics with clear quantised conductance plateaus up to $6(2e^2/h)$. On the other hand p-Ge provided us a system that enabled us to explore many body effects in these systems. One dimensional transport in holes is remarkably rich and broad and the measurements reported here have already provided us with new effects, such as the 0.25 G_0 plateau, which on application of an in-plane magnetic field clearly splits into two, implying that it is spin degenerate. Although we have tried to provide a couple of explanations, it is still not explicable clearly on the basis of any known many body interactions. Further measurements are needed on very low disorder and low carrier concentration hole gases. It is also a fairly new system with a potential of opening the spintronics field to p-Ge.

In this project we have laid the ground work for creating complex devices using both $In_{0.75}Ga_{0.25}As$ and p-Ge to be used for spintronics.

Appdendix

Processing steps for InGaAs Devices

1. **Cleaving the sample:** making short scribes at the end of the wafer to define the chip size, then cleaving: the chip will cleave along the Major axis (high mobility direction).

2. **Cleaning the sample: a)** Put the sample in a plastic beaker with acetone, put in Sonicator for roughly 5 minutes **b)** Rinse in a plastic beaker or petri dish with propanol (IPA) and put in Solicitor for 5 mins and dry with nitrogen gun.

3. **Etch solution:** Make up your Etch Solution by mixing **1:8:120 - H_2SO_4:H_2O_2:H_2O** (Etch rate 6nm/s) in a plastic beaker. Leave it to stabilise for at least 1 hour.

4. **Mesa patterning:** Pre-bake sample on hotplate at 125 °C for about 10 minutes and then spin Shipley 'Microposit 1805' at 5500 r/min for 45sec (0.5 μm thick); post bake for 60 seconds at 115 °C

5. Expose the Mesa pattern (J11 Mask) with optical mask aligner for 3.5 sec (being very careful to align the mask mesa pattern to the cleaved crystal direction.

6. Develop with MF 319 Developer for 42 seconds, rinsing in clean DI water, drying with N2.

7. Check the thickness of the resist with a Dektak

8. **Wet etching:** 1:8:120 **H_2SO_4:H_2O_2:H_2O** for roughly 40 seconds to get about 180nm deep. (depends on the etching rate of the etch) checking hight after 15 sec with the Dektak), desired etching depth: just down to the 2DEG (150nm-200nm for InGaAs wafers.)

9. Remove resist with acetone, rinsing with propanol, and dry with N2

10. Check the thickness of the mesa with a Dektak

11. Spin Shipley 'Microposit 1813' at 5500 r/min for 45 sec, bake for 1 min at 115 °C

12. Expose the Ohmic pads (available on J11 Mask) with optical mask aligner for 6.5 sec (being very careful to align the mask ohmic pattern to the mesa)

13. Lay the chip in Chlorobenzene for 1.5 min (that hardens the top of the resist for an undercut) , rinsing in clean! DI water, drying with N2

14. Develop with MF 319 Developer for 1.5 mins, rinsing in clean! DI water, drying with N2

15. Remove the oxide surface layer with a 40% HF acid for 10 sec, rinsing in clean! DI water, drying with N2. Make sure there is someone present in the room in case of emergency and wear the proper HF gear being extra careful.

16. **Ohmic evaporation** Evaporate AuGeNi slugs (0.5g gives a thickness of 150nm), it is important that the slugs are evaporated completely, that means the rate at the crystal must be really! Zero.

17. Lift-off in acetone for a minimum of 10 min or overnight, using a pipette to blow off the metal from the sample, put the sample out and squeeze acetone onto the sample to remove remaining metal, rinsing with propanol, drying with N2, check that there is no ohmic material left with a microscope while in IPA solution. (do no use the microscope in acetone solution).

18. **Anneal contacts:** use of rapid thermal annealer, profile: 30 sec at 220 °C, 80 sec at 430 °C, 30 sec at 220 °C; doing some learn cycles before annealing real sample, you can use SF01 available on the filesystem. or Ken01.

19. Check ohmic contacts with the prober: at room temperature they should have a resistance of roughly 30 kOhms (depends on electron density and sample geometry, but the resistance should be less than 100 kOhms), use liquid N2 (in the dark) to cool the sample (the resistance *must!* drop below 10 kOhms (if not another annealing process can help).

SiOx deposition

1. Pack the samples in a membrane case and leave it to Dave Ellis's pigeon hole, or whoever is in charge of the PECVD and email him the thickness required. 50nm is working well.

2. Once the SiOx deposition is complete, Pre-bake sample on hotplate at 125 °C for about 10 minutes and then spin Shipley 'Microposit 1813' at 5500 r/min for 45sec (0.5 μm thick); baking 60 sec at 115 °C

3. Expose the ohmic pads (J11 Mask) with optical mask aligner for 6.5 sec (being very careful to align the mask mesa ohmic pads to the Mesa pattern.

4. Develop with MF 319 Developer for 50 seconds, rinsing in clean DI water, drying with N2.

5. remove SiOx from the ohmic pads with a 40% dip HF acid for 15 sec (this should etch 50nm of SiOx and make windows for the ohmic contacts), rinsing in clean! DI water, drying with N2. Make sure there is someone present in the room in case of emergency and wear the proper HF gear being extra careful.

Preparing for EBL gates

1. Using a Asher, Ash sample in ozone plasma for 1 minute, then dip in 10% HCL solution for 10 seconds and rinse in DI water and use a Weir to clean, then rinse in acetone and then IPA.

2. Bake in Oven at 150 °C for 10 minutes.

3. **1st layer:** Spin "100K A6 1-1 ANISOLE" at 8000rpm for 60seconds and bake at hot plate for 3 min at 180°C.

4. **2nd layer:** Spin "950K A11 MIBK 1:5" at 8000rpm for 60s and bake on hot plate for 3 min at 180°C.

5. The sample is now ready for E-beam, finalise your design on Autocad and send to ebeam@sp.phy.cam.ac.uk.

Evaporating E-beam Gates

1. Develop sample for 8 seconds in fast developer MEK:MIBK:IPA 1:5:15, and rinse in IPA for 15 seconds than dip in 10% HCL and rinse in DI water in Weir.
2. Make sure that the E-beam gates are exposed correctly and once happy you can evaporate the gates.
3. Evaporate 7.5 nm of Ti and 17.5 nm of Au make sure you do it in high vacuum usually 4 x 10^{-7} bar.
4. Once evaporation is done, keep in Acetone overnight in sealed container and lift off the next morning using a pipette and blow gently.

Processing steps for optical gates

1. Using an asher, ash sample in ozone plasma for 1 minute, then dip in 20% HCL solution for 20 seconds and rinse in DI water and use a Weir to clean, then rinse in acetone and then IPA.
2. Spin LOR7B at 3000rpm for 50s and post bake on hot plate for 10min at 175°C.
3. Spin Shipley 'Microposit 1805' at 3000 r/min for 30sec, bake for 1 min at 115 °C
4. Expose Optical gates at UV using J Mask 11 for 3.5 sec and develop in MF319 for 35 sec.
5. Dip in 20% HCL solution for 20s and rinse in DI Water.
6. Evaporate 20nm Ti and 130 nm Au.
7. Once Evaporation is done, leave in SVC14 solution for 10 min on hot plate at 80°C. and lift off using a pipette.

Processing steps for optical gates for dog-bone

1. Spin Shipley 'Microposit 1813' at 5500 r/min for 45 sec (1.2 μm thick); postbake 1 min at 115 °C
2. Expose with optical mask aligner for 6.5 sec for optical gates
3. Lay the chip in chlorobenzene for 2min (hardens the top of the resist for an undercut) , rinsing in clean! DI water, drying with N2

4. Develop with MF 319 Developer for 50 sec, rinsing in clean! DI water, drying with N2

5. removing oxide surface layer with a diluted HCl dip: H2O:HCl (10:1) for 15 sec, rinsing in clean! DI water, drying with N2

6. evaporate Ti/AU (20nm/60nm), make sure that the evaporation chamber is clean if not clean, hoover with a vacuum cleaner.

7. lift-off in acetone overnight; using a pipette to blow off the metal from the sample, put the sample out and squeeze acetone onto the sample to remove remaining metal, rinsing with propanol, drying with N2

Processing steps for optical gates with top gate (dogbone)

1. spinning Shipley 'Microposit 1813' at 5500 r/min for 45 sec (1.2 μm thick); baking 1 min at 115 °C

2. exposure the optical gates with optical mask aligner for 6.5 sec, then align the dogbone to the the mesa structure and expose for 6.5 seconds.

3. developing with MF 319 Developer for 50 sec, rinsing in clean! DI water, drying with N2

4. Lay the chip in Chlorobenzene for 2min (hardens the top of the resist for an undercut) , rinsing in clean! DI water, drying with N2

5. Develop with MF 319 Developer for 55 sec, rinsing in clean! DI water, drying with N2

6. removing oxide surface layer with a diluted HCl dip: H2O:HCl (3:1) for 15 sec, rinsing in clean! DI water, drying with N2

7. evaporat4 Ti/AU (20nm/60nm), make sure that the evaporation chamber is clean if not clean, hoover with a vacuum cleaner.

8. lift-off in acetone overnight; using a pipette to blow off the metal from the sample, put the sample out and squeeze acetone onto the sample to remove remaining metal, rinsing with propanol, drying with N2

Packaging

1. scribe and snap into individual devices
2. use GE varnish to attach to sample holder
3. bond into prepared sample holder

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